VLSI Testing

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IC Design & Production Flow

1. Design House → IC Design & Design-for-Test

2. Foundry → Wafer Manufacturing

3. Foundry or Testing House → Wafer Testing

4. Packaging House → Packaging

5. Testing House → Final Testing

→ Shipping
Course Objectives

To learn about

- The role and cost of testing in VLSI circuits & systems
- The types of faults expected and how to model them
- Fundamental techniques for detecting defects in VLSI circuits
- Algorithms for automatic test generation
- Schemes for designing circuits to be easily testable and/or with self-test capability
- Hands-on experience with state-of-the-art computer-aided-test tools in the laboratory
- How to survey state-of-the-art research topic
Contents

- Introduction
- Fault Simulation
- Test Generation
- Design for Testability
- Built-in-Self-Test
- Test Compression
- Memory Testing
- Boundary Scan
- Cored-based & SOC Testing
- Special topics
References


4. Proceedings in $\geq 30$ IEEE Conferences/Symposiums/Workshops on testing each year.

Class Requirements & Grading

Prerequisite: Logic design, Electonics I & II, Electrical Circuits, Basic VLSI design concepts

- Homework & Exercises 20-35%
- Midterm & Final Exams 50-60%
- Final Project 20-30%

Teaching Assistants:
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