Cell-Based IC Physical Design & Verification

SOC Encounter

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VLSI System Design

Reference: SOC Encounter Training Manual, 2007, edited by CIC.

Introduction

- We’ll use some EDA tools to transform synthesized design to layout
- Tools
  - SOC Encounter: Floorplanningand APR
  - icfb: Cell replacement with layout
  - Calibre: DRC, LVS

Prepare File

- Unix% cp -r /home4/classuser/sys0701/sys0701ta1/SOCE .
- Library
  - Physical Library (.lef)
  - Timing Library (.lib)
- User Data
  - Gate-Level netlist (.v)
  - SDC constraints (.sdc)
  - IO constraint (.ioc)

Gate-Level netlist (1/3)

- Synthesized RTL code

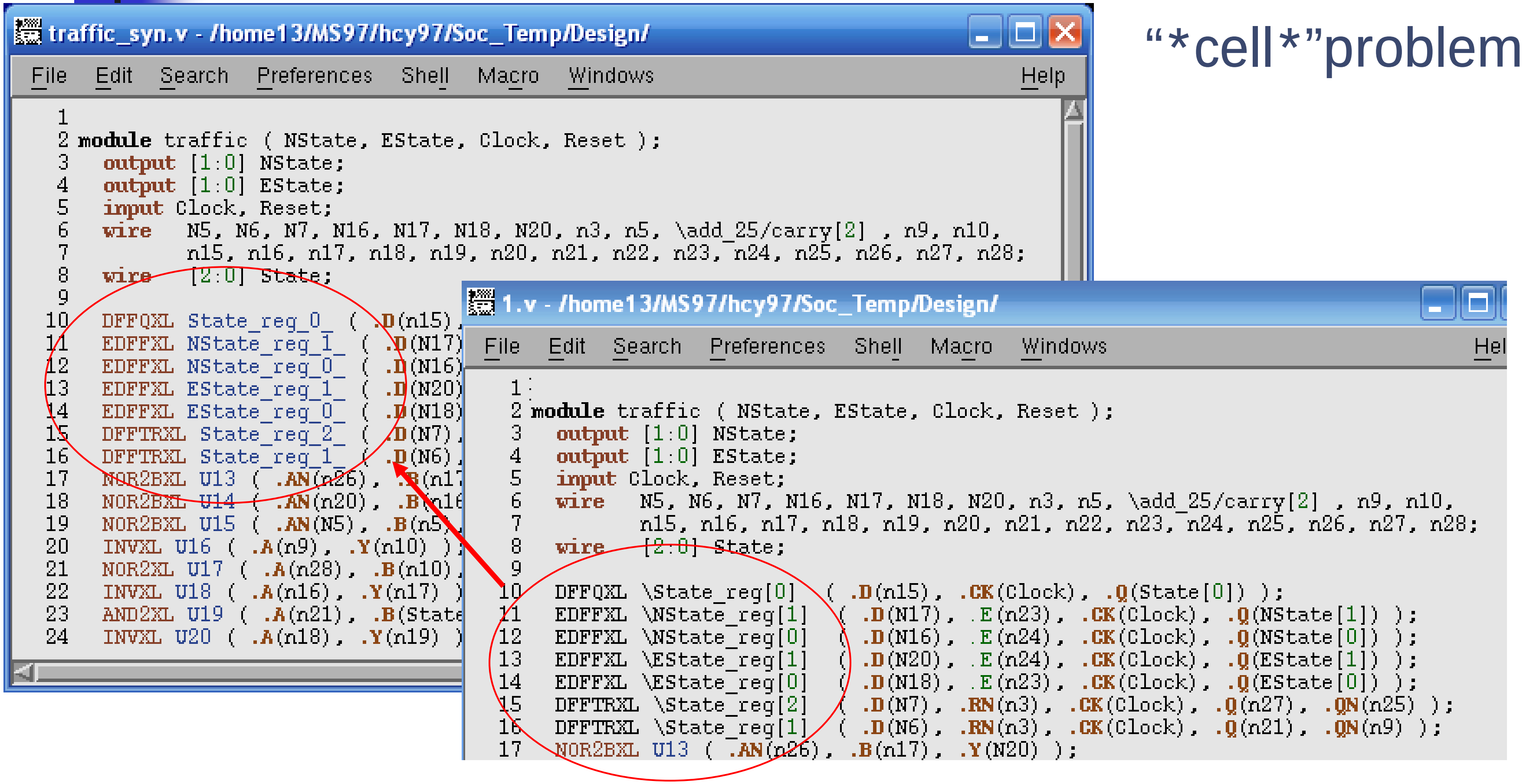
  –“assign”statement is not allowed.

  To solve this, typing

  “set_fix_multiple_port_nets–all –buffer_constants” in command window before compile.

  –“*cell*”problem. To solve this, “change_names –rule verilog–verbose -hierarchy” in command window after compile.

Gate-Level netlist (2/3)

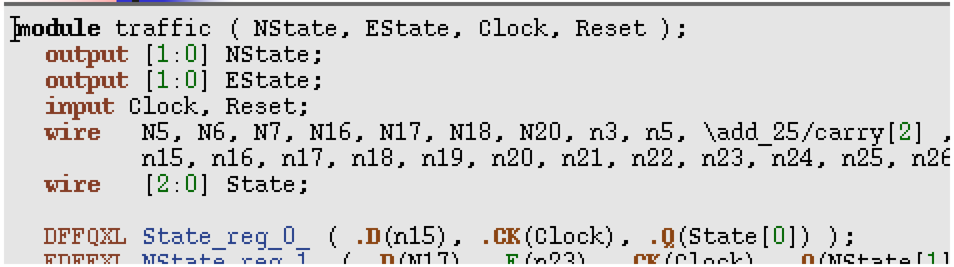


```
module traffic ( NState, EState, Clock, Reset );
  output [1:0] NState;
  output [1:0] EState;
  input Clock, Reset;
  wire   N5, N6, N7, N16, N17, N18, N20, n3, n5, \add_25/carry[2] , n9, n10,
         n15, n16, n17, n18, n19, n20, n21, n22, n23, n24, n25, n26, n27, n28;
  wire   [2:0] State;

  DFFQXL State_reg_0_  ( .D(n15),
  EDFFXL NState_reg_1_  ( .D(N17)
  EDFFXL NState_reg_0_  ( .D(N16)
  EDFFXL EState_reg_1_  ( .D(N20)
  EDFFXL EState_reg_0_  ( .D(N18)
  DFFTRXL State_reg_2_  ( .D(N7),
  DFFTRXL State_reg_1_  ( .D(N6),
  NOR2BXL U13 ( .AN(n26), .B(n17
  NOR2BXL U14 ( .AN(n20), .B(n16
  NOR2BXL U15 ( .AN(N5), .B(n5),
  INVXL U16 ( .A(n9), .Y(n10) );
  NOR2XL U17 ( .A(n28), .B(n10),
  INVXL U18 ( .A(n16), .Y(n17) )
  AND2XL U19 ( .A(n21), .B(State
  INVXL U20 ( .A(n18), .Y(n19) )
```

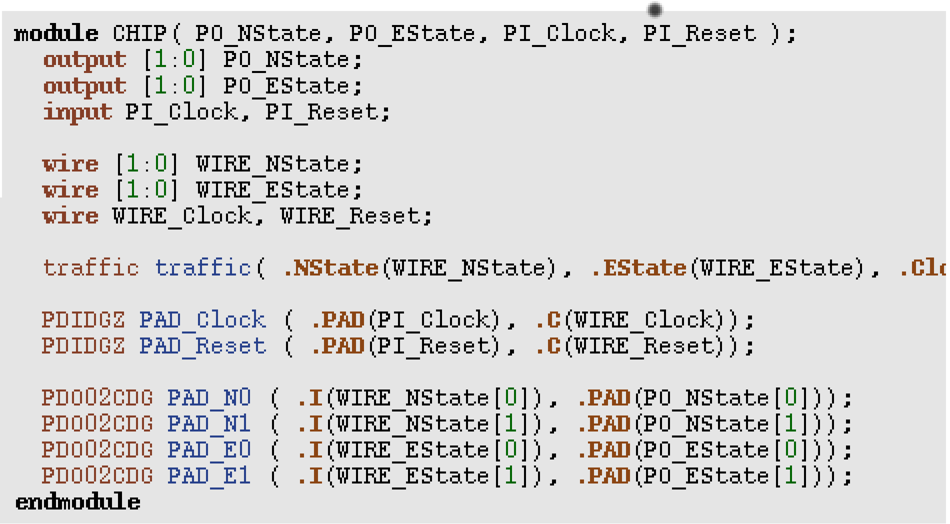
```
module traffic ( NState, EState, Clock, Reset );
  output [1:0] NState;
  output [1:0] EState;
  input Clock, Reset;
  wire   N5, N6, N7, N16, N17, N18, N20, n3, n5, \add_25/carry[2] , n9, n10,
         n15, n16, n17, n18, n19, n20, n21, n22, n23, n24, n25, n26, n27, n28;
  wire   [2:0] State;

  DFFQXL \State_reg[0]  ( .D(n15), .CK(Clock), .Q(State[0]) );
  EDFFXL \NState_reg[1]  ( .D(N17), .E(n23), .CK(Clock), .Q(NState[1]) );
  EDFFXL \NState_reg[0]  ( .D(N16), .E(n24), .CK(Clock), .Q(NState[0]) );
  EDFFXL \EState_reg[1]  ( .D(N20), .E(n24), .CK(Clock), .Q(EState[1]) );
  EDFFXL \EState_reg[0]  ( .D(N18), .E(n23), .CK(Clock), .Q(EState[0]) );
  DFFTRXL \State_reg[2]  ( .D(N7), .RN(n3), .CK(Clock), .Q(n27), .QN(n25) );
  DFFTRXL \State_reg[1]  ( .D(N6), .RN(n3), .CK(Clock), .Q(n21), .QN(n9) );
  NOR2BXL U13 ( .AN(n26), .B(n17), .Y(N20) );
```

"*cell*"problem

Gate-Level netlist (3/3)

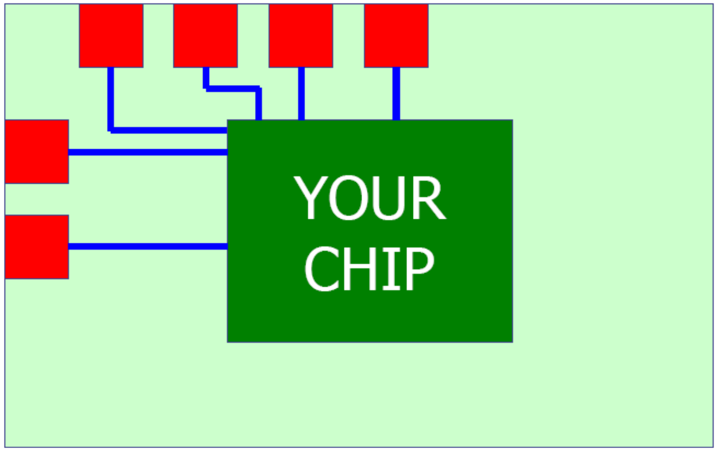


```
module traffic ( NState, EState, Clock, Reset );
  output [1:0] NState;
  output [1:0] EState;
  input Clock, Reset;
  wire    N5, N6, N7, N16, N17, N18, N20, n3, n5, \add_25/carry[2] ,
          n15, n16, n17, n18, n19, n20, n21, n22, n23, n24, n25, n26
  wire    [2:0] State;

  DFFQXL State_reg_0_ ( .D(n15), .CK(Clock), .Q(State[0]) );
  EDFFXL NState_reg_1_  ( .D(N17), .E(n23), .CK(Clock), .Q(NState[1]
```



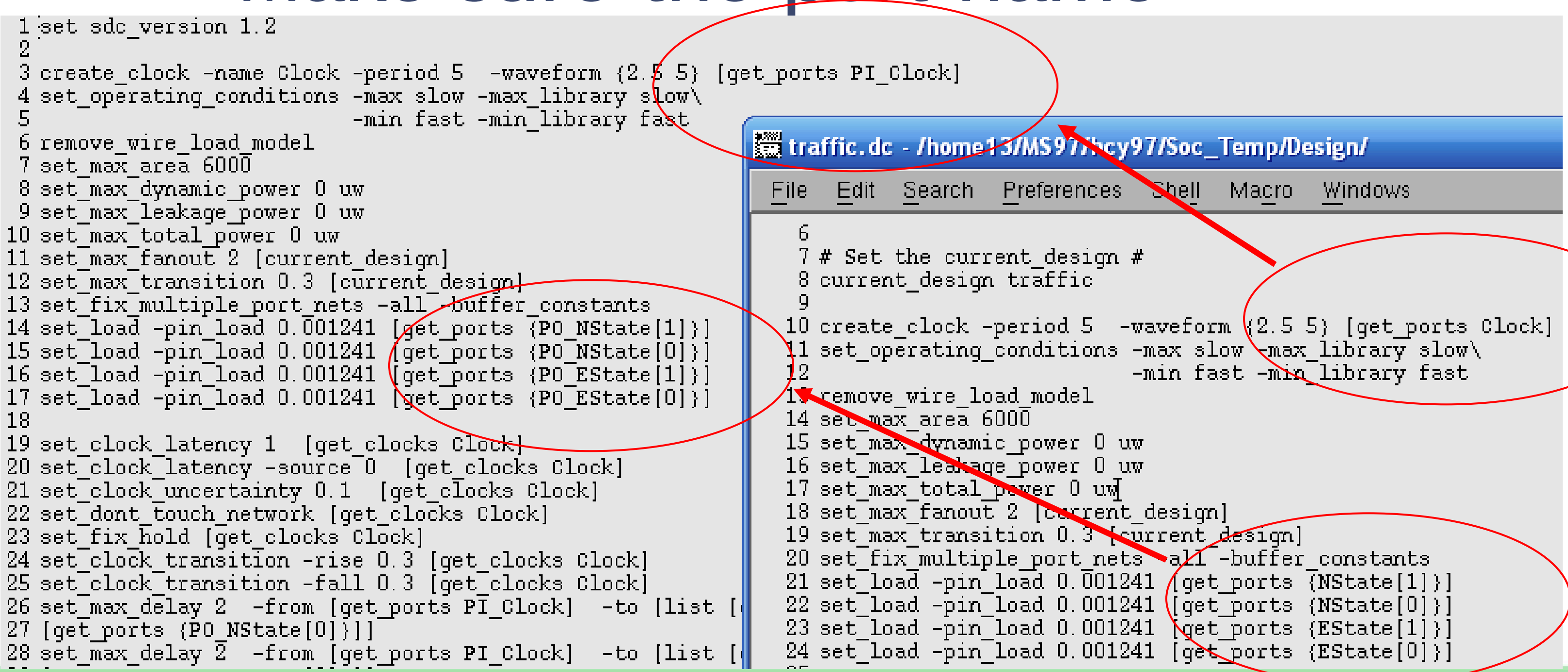
```
module CHIP( PO_NState, PO_EState, PI_Clock, PI_Reset );
  output [1:0] PO_NState;
  output [1:0] PO_EState;
  input PI_Clock, PI_Reset;

  wire [1:0] WIRE_NState;
  wire [1:0] WIRE_EState;
  wire WIRE_Clock, WIRE_Reset;

  traffic traffic( .NState(WIRE_NState), .EState(WIRE_EState), .Clo

  PDIDGZ PAD_Clock ( .PAD(PI_Clock), .C(WIRE_Clock));
  PDIDGZ PAD_Reset ( .PAD(PI_Reset), .C(WIRE_Reset));

  PDO02CDG PAD_N0  ( .I(WIRE_NState[0]), .PAD(PO_NState[0]));
  PDO02CDG PAD_N1  ( .I(WIRE_NState[1]), .PAD(PO_NState[1]));
  PDO02CDG PAD_E0  ( .I(WIRE_EState[0]), .PAD(PO_EState[0]));
  PDO02CDG PAD_E1  ( .I(WIRE_EState[1]), .PAD(PO_EState[1]));
endmodule
```

- When Verilogfile is ready
  - Put all verilogfile (CHIP.v) into SOC_tutor/vlog
- Adding I/O pads into CHIP.v
  - input pad ：PDIDGZ
  - output pad ：PDO02CDG



SDC Constraint

- Make use of the dc constraint
- Make sure the port name

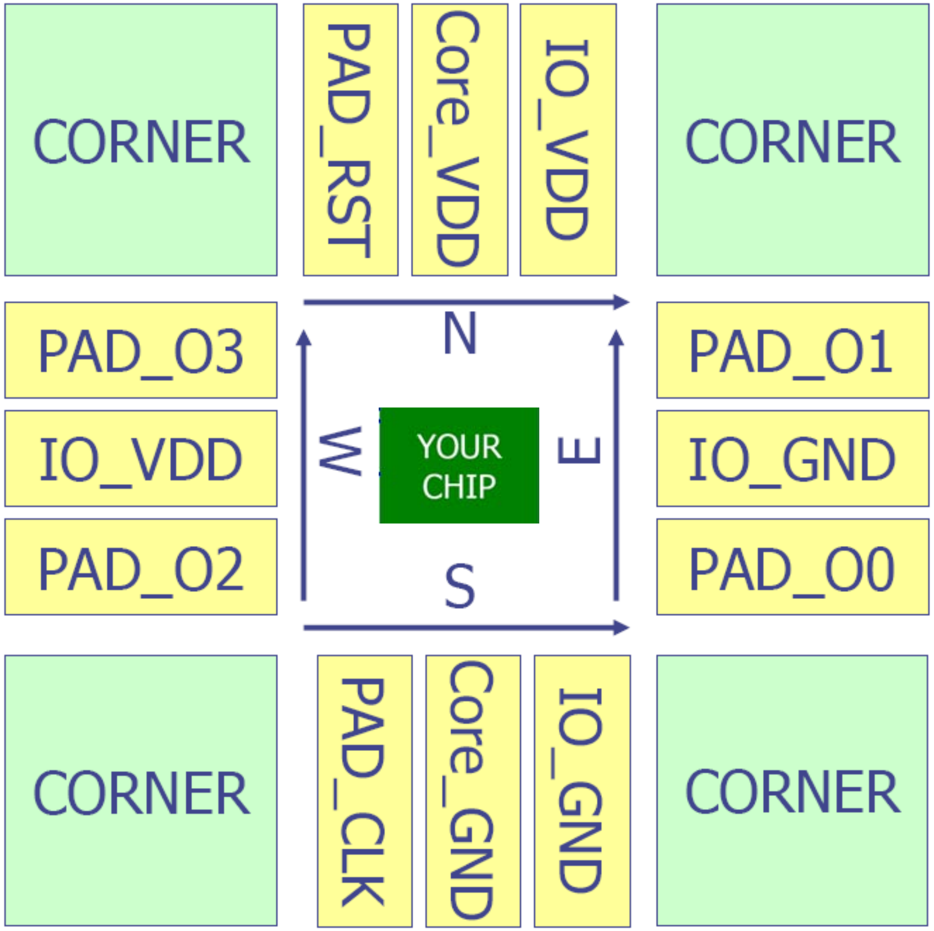


```
set sdc_version 1.2

create_clock -name Clock -period 5  -waveform {2.5 5} [get_ports PI_Clock]
set_operating_conditions -max slow -max_library slow\
                         -min fast -min_library fast
remove_wire_load_model
set_max_area 6000
set_max_dynamic_power 0 uw
set_max_leakage_power 0 uw
set_max_total_power 0 uw
set_max_fanout 2 [current_design]
set_max_transition 0.3 [current_design]
set_fix_multiple_port_nets -all -buffer_constants
set_load -pin_load 0.001241 [get_ports {PO_NState[1]}]
set_load -pin_load 0.001241 [get_ports {PO_NState[0]}]
set_load -pin_load 0.001241 [get_ports {PO_EState[1]}]
set_load -pin_load 0.001241 [get_ports {PO_EState[0]}]

set_clock_latency 1  [get_clocks Clock]
set_clock_latency -source 0  [get_clocks Clock]
set_clock_uncertainty 0.1  [get_clocks Clock]
set_dont_touch_network [get_clocks Clock]
set_fix_hold [get_clocks Clock]
set_clock_transition -rise 0.3 [get_clocks Clock]
set_clock_transition -fall 0.3 [get_clocks Clock]
set_max_delay 2  -from [get_ports PI_Clock]  -to [list [
[get_ports {PO_NState[0]}]]
set_max_delay 2  -from [get_ports PI_Clock]  -to [list [
```

traffic.dc - /home13/MS97/hcy97/Soc_Temp/Design/

```

# Set the current_design #
current_design traffic

create_clock -period 5  -waveform {2.5 5} [get_ports Clock]
set_operating_conditions -max slow -max_library slow\
                         -min fast -min_library fast
remove_wire_load_model
set_max_area 6000
set_max_dynamic_power 0 uw
set_max_leakage_power 0 uw
set_max_total_power 0 uw
set_max_fanout 2 [current_design]
set_max_transition 0.3 [current_design]
set_fix_multiple_port_nets -all -buffer_constants
set_load -pin_load 0.001241 [get_ports {NState[1]}]
set_load -pin_load 0.001241 [get_ports {NState[0]}]
set_load -pin_load 0.001241 [get_ports {EState[1]}]
set_load -pin_load 0.001241 [get_ports {EState[0]}]
```

IO Constraint (1/3)



IO Constraint (2/3)

Pad: CORNER0	NW	Pad: CORNER2	SE
Pad: PAD_RESET	N	Pad: PAD_CLK	S
Pad: PAD_CoreVDD	N	Pad: PAD_CoreVSS	S
Pad: PAD_IOVDD1	N	Pad: PAD_IOGND1	S

Pad: CORNER1	NE	Pad: CORNER3	SW
Pad: PAD_O2	W	Pad: PAD_O0	E
Pad: PAD_IOVDD	W	Pad: PAD_IOVSS	E
Pad: PAD_O3	W	Pad: PAD_O1	E

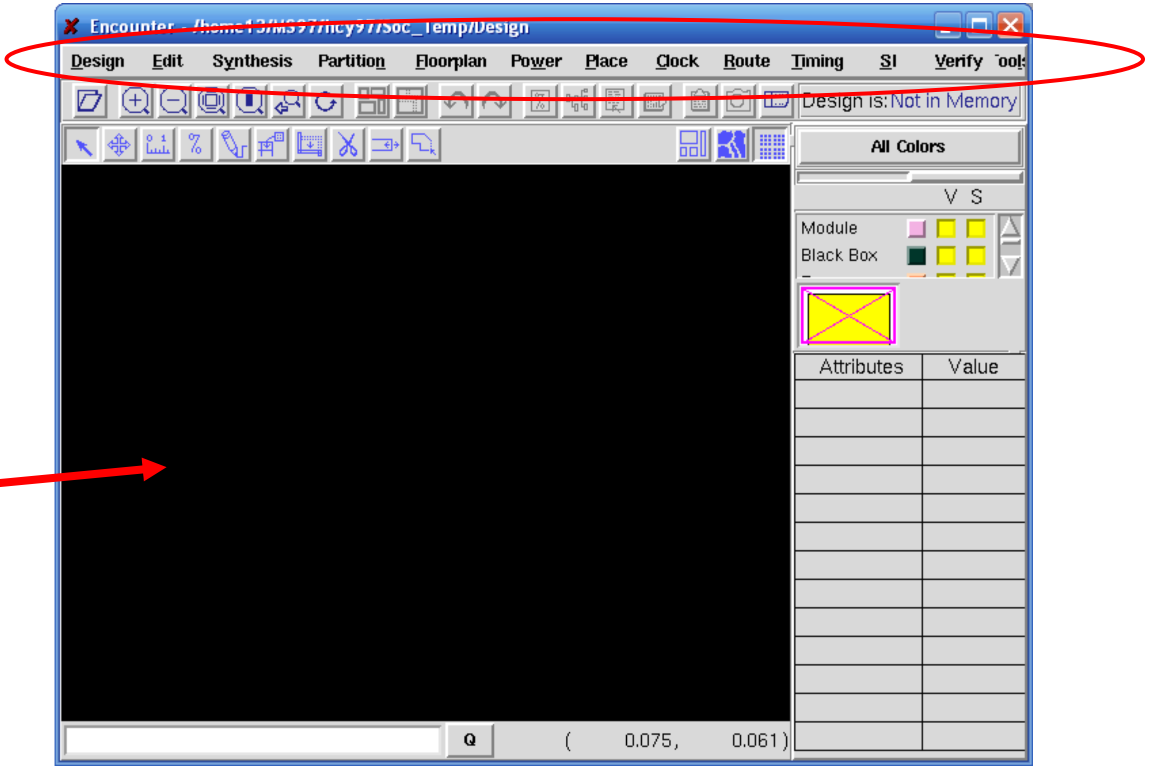
IO Constraint (3/3)

Pad: CORNER0	NW	PCORNERDGZ
Pad: PAD_CoreVDD	N	PVDD1DGZ
Pad: PAD_CoreVSS	S	PVSS1DGZ
Pad: PAD_IOVDD	S	PVDD2DGZ
Pad: PAD_IOVSS	E	PVSS2DGZ

Put a pair of PAD POWER PAD about every 7 I/O pads.

Starting SOC Encounter

- In /SOC_tutor directory, type "encounter"



Design is: Not in Memory

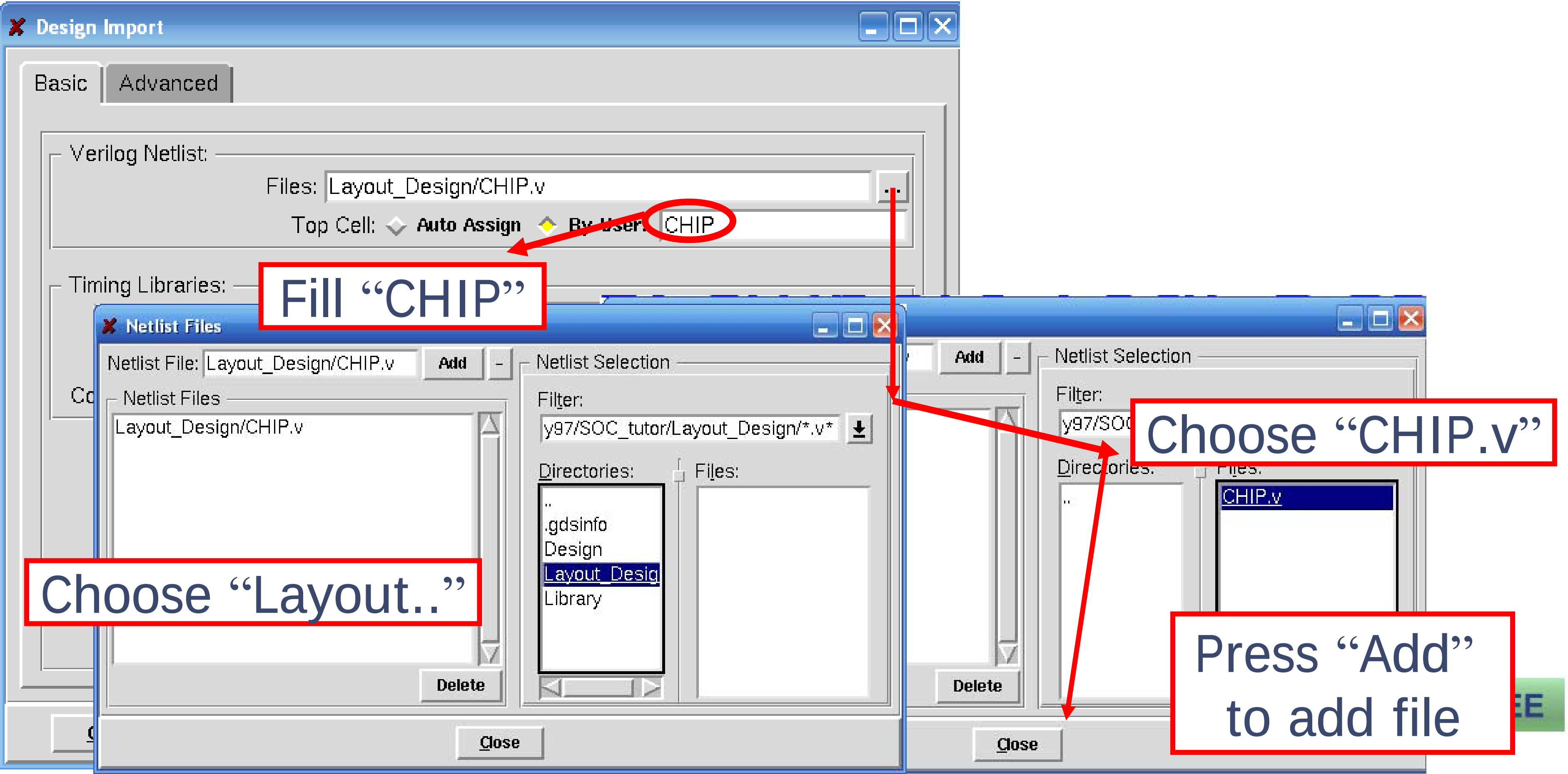
(0.075, 0.061)

Menu bar

Artwork window

Import Your Design (1/6)

- Design → Design Import



Fill “CHIP”

Choose “CHIP.v”

Choose “Layout..”

Press “Add” to add file

Design Import

Verilog Netlist:

Files: Layout_Design/CHIP.v

Top Cell: ○ Auto Assign ● By User: CHIP

Netlist Files

Netlist File: Layout_Design/CHIP.v

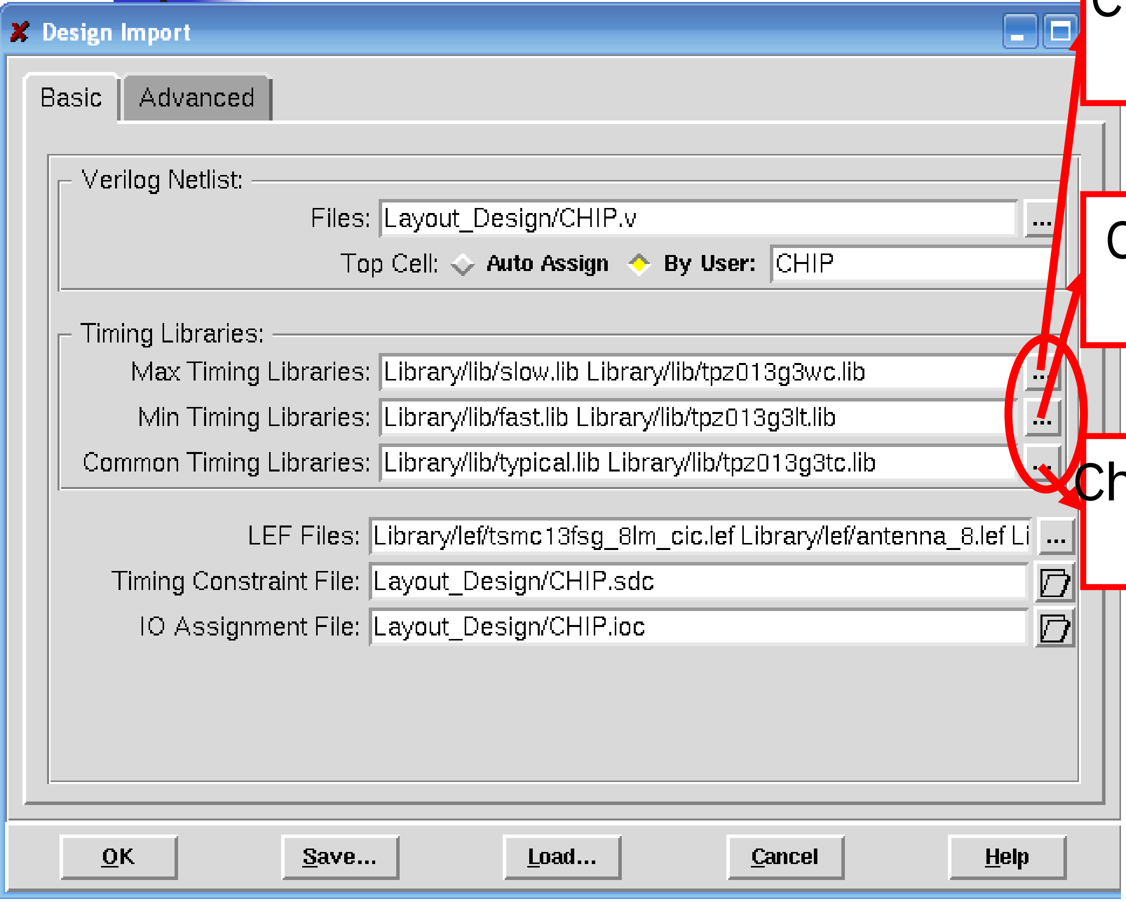
Netlist Files: Layout_Design/CHIP.v

Filter: y97/SOC_tutor/Layout_Design/*.v*

Directories: .. .gdsinfo Design Layout_Desig Library

Files: CHIP.v

Import Your Design (2/6)



Design Import

Verilog Netlist:

Files: Layout_Design/CHIP.v

Top Cell: ◇ Auto Assign ◆ By User: CHIP

Timing Libraries:

Max Timing Libraries: Library/lib/slow.lib Library/lib/tpz013g3wc.lib

Min Timing Libraries: Library/lib/fast.lib Library/lib/tpz013g3lt.lib

Common Timing Libraries: Library/lib/typical.lib Library/lib/tpz013g3tc.lib

LEF Files: Library/lef/tsmc13fsg_8lm_cic.lef Library/lef/antenna_8.lef Li

Timing Constraint File: Layout_Design/CHIP.sdc

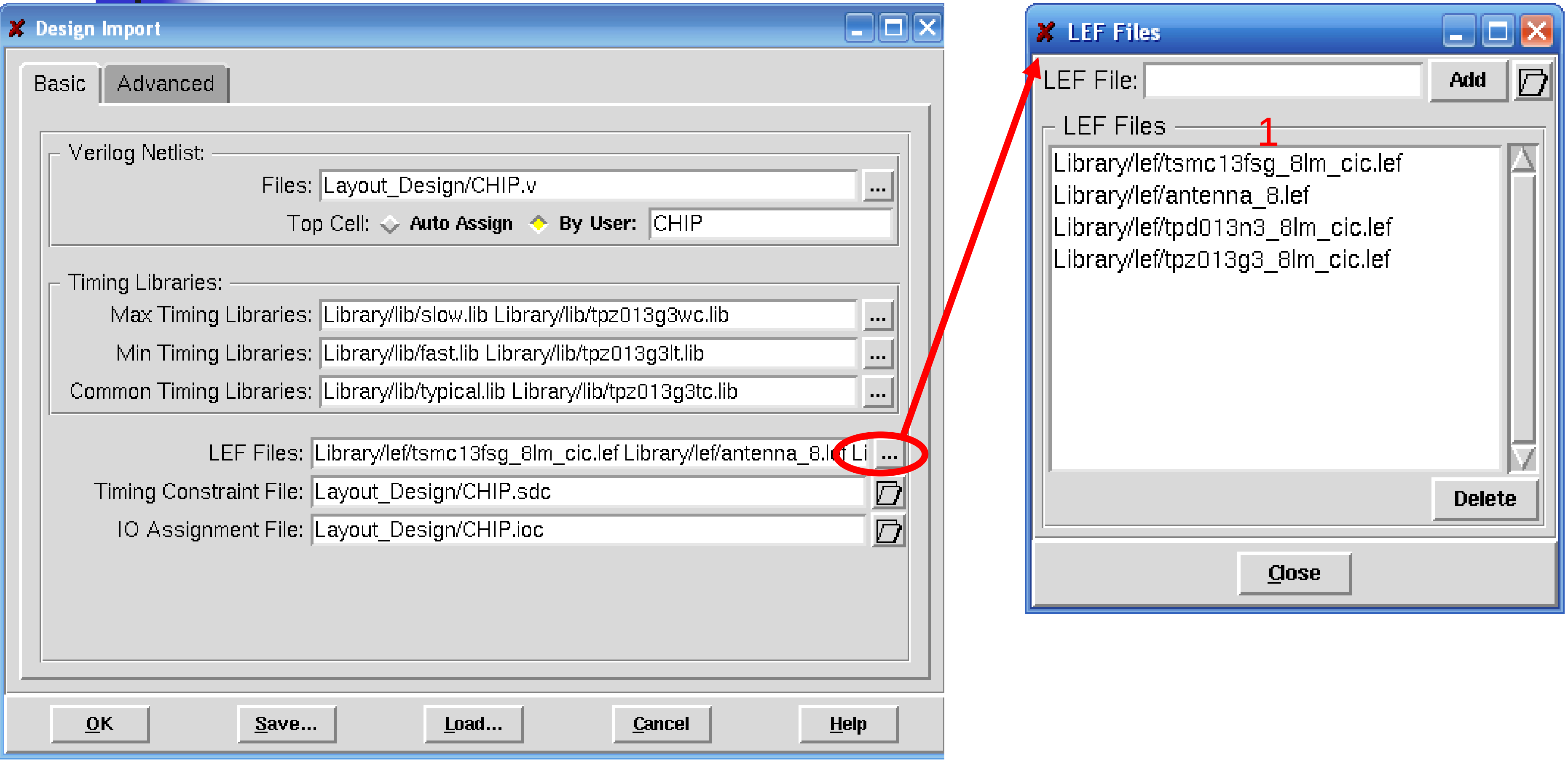
IO Assignment File: Layout_Design/CHIP.ioc

Choose “Library/lib/slow.lib” and “Library/lib/tpz013g3wc.lib”

Choose “Library/lib/fast.lib” and “Library/lib/tpz013lt.lib”

Choose “Library/lib/typical.lib” and “Library/lib/tpz013g3tc.lib”

Import Your Design (3/6)



Design Import

Verilog Netlist:

Files: Layout_Design/CHIP.v

Top Cell: ◇ Auto Assign ◆ By User: CHIP

Timing Libraries:

Max Timing Libraries: Library/lib/slow.lib Library/lib/tpz013g3wc.lib

Min Timing Libraries: Library/lib/fast.lib Library/lib/tpz013g3lt.lib

Common Timing Libraries: Library/lib/typical.lib Library/lib/tpz013g3tc.lib

LEF Files: Library/lef/tsmc13fsg_8lm_cic.lef Library/lef/antenna_8.lef Li

Timing Constraint File: Layout_Design/CHIP.sdc

IO Assignment File: Layout_Design/CHIP.ioc

LEF Files

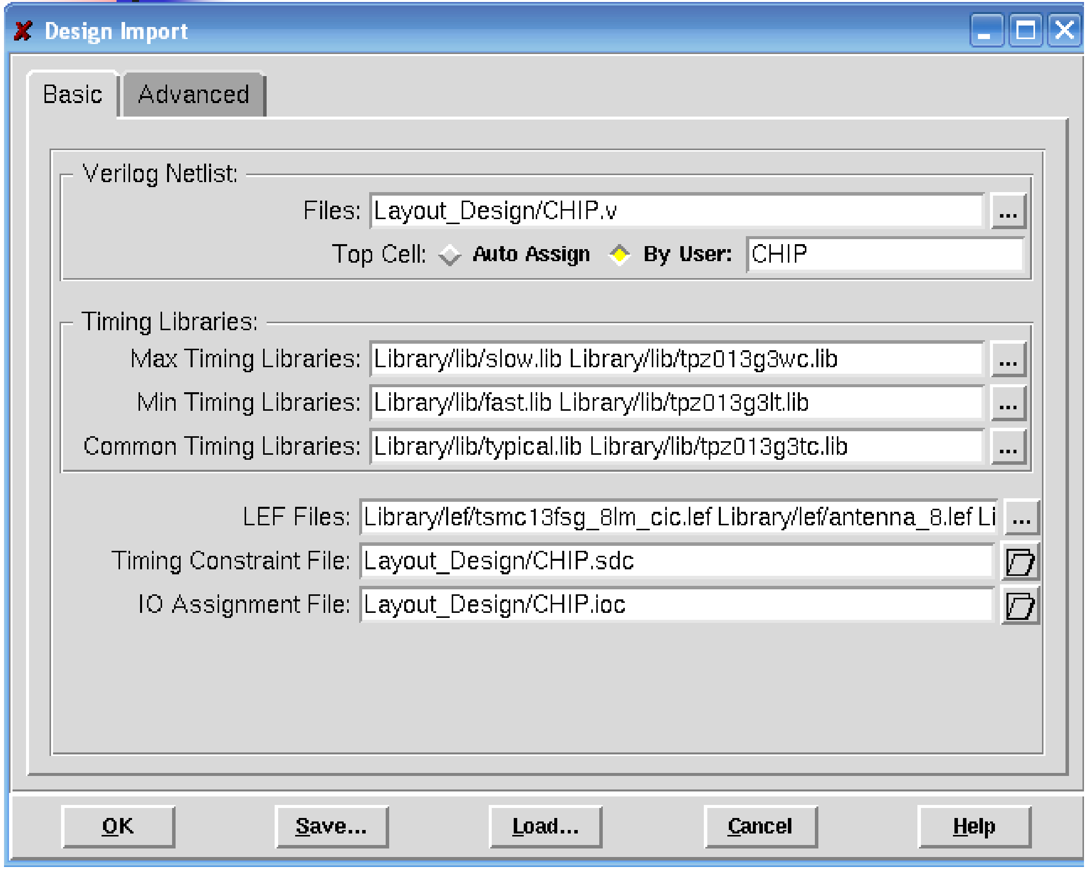
LEF File:

LEF Files

1

Library/lef/tsmc13fsg_8lm_cic.lef
Library/lef/antenna_8.lef
Library/lef/tpd013n3_8lm_cic.lef
Library/lef/tpz013g3_8lm_cic.lef

Import Your Design (4/6)



Design Import

Verilog Netlist:

Files: Layout_Design/CHIP.v

Top Cell: ○ Auto Assign ● By User: CHIP

Timing Libraries:

Max Timing Libraries: Library/lib/slow.lib Library/lib/tpz013g3wc.lib

Min Timing Libraries: Library/lib/fast.lib Library/lib/tpz013g3lt.lib

Common Timing Libraries: Library/lib/typical.lib Library/lib/tpz013g3tc.lib

LEF Files: Library/lef/tsmc13fsg_8lm_cic.lef Library/lef/antenna_8.lef Li

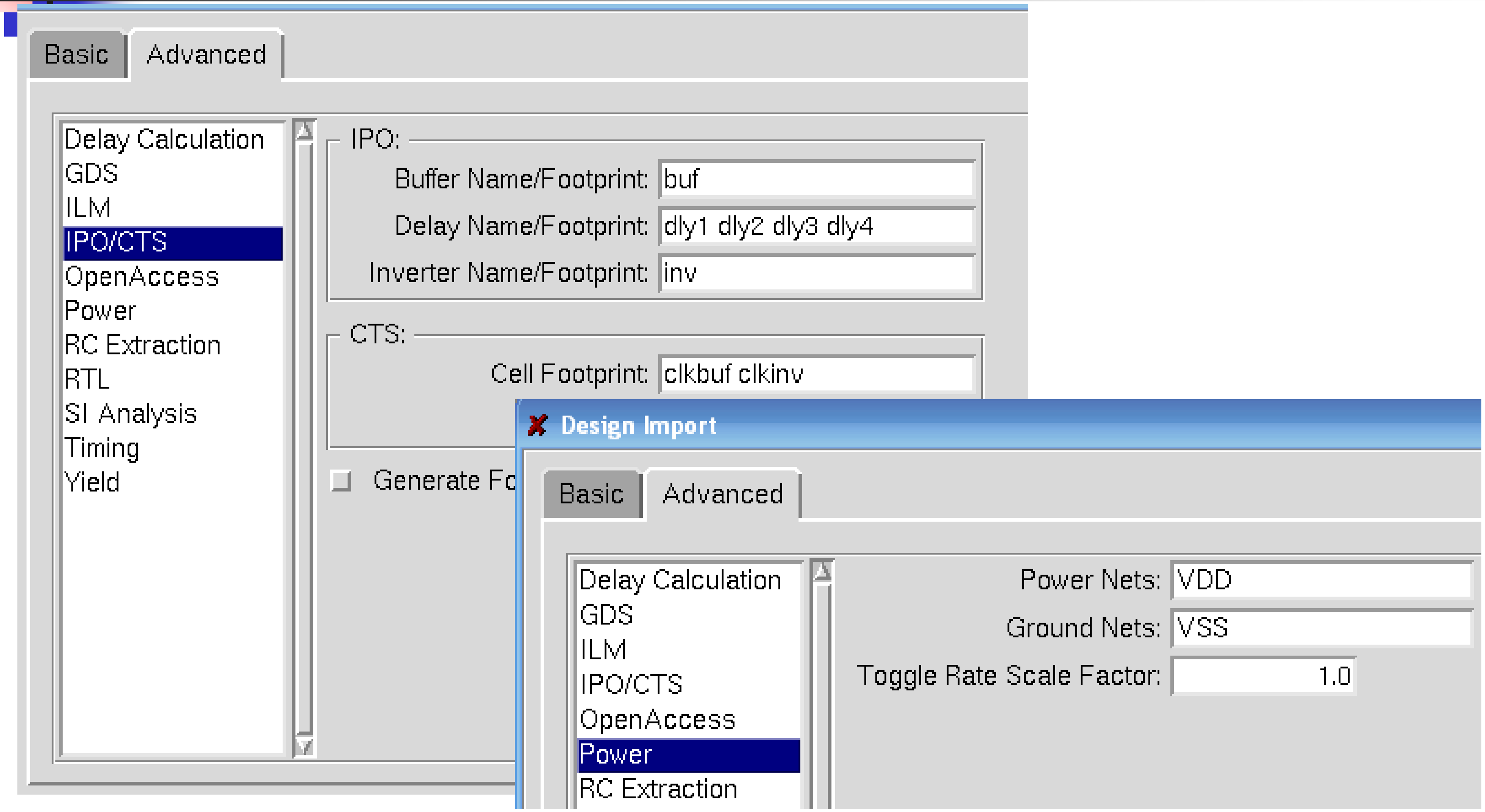
Timing Constraint File: Layout_Design/CHIP.sdc

IO Assignment File: Layout_Design/CHIP.ioc

CHIP.sdc & CHIP.ioc :

Layout_Design/

Import Your Design (5/6)



IPO:

Buffer Name/Footprint: buf

Delay Name/Footprint: dly1 dly2 dly3 dly4

Inverter Name/Footprint: inv

CTS:

Cell Footprint: clkbuf clkinv

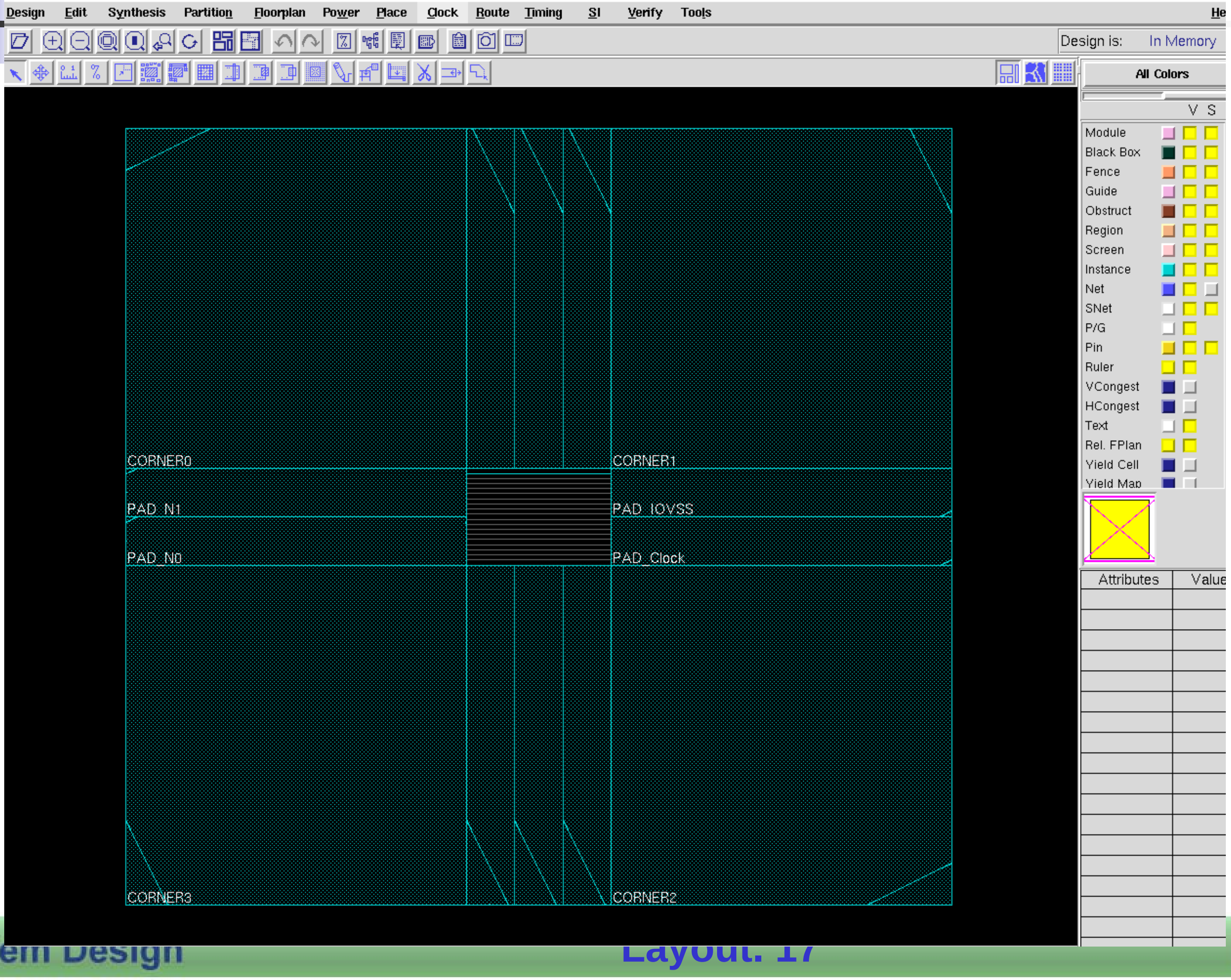
□ Generate Fo

Power Nets: VDD

Ground Nets: VSS

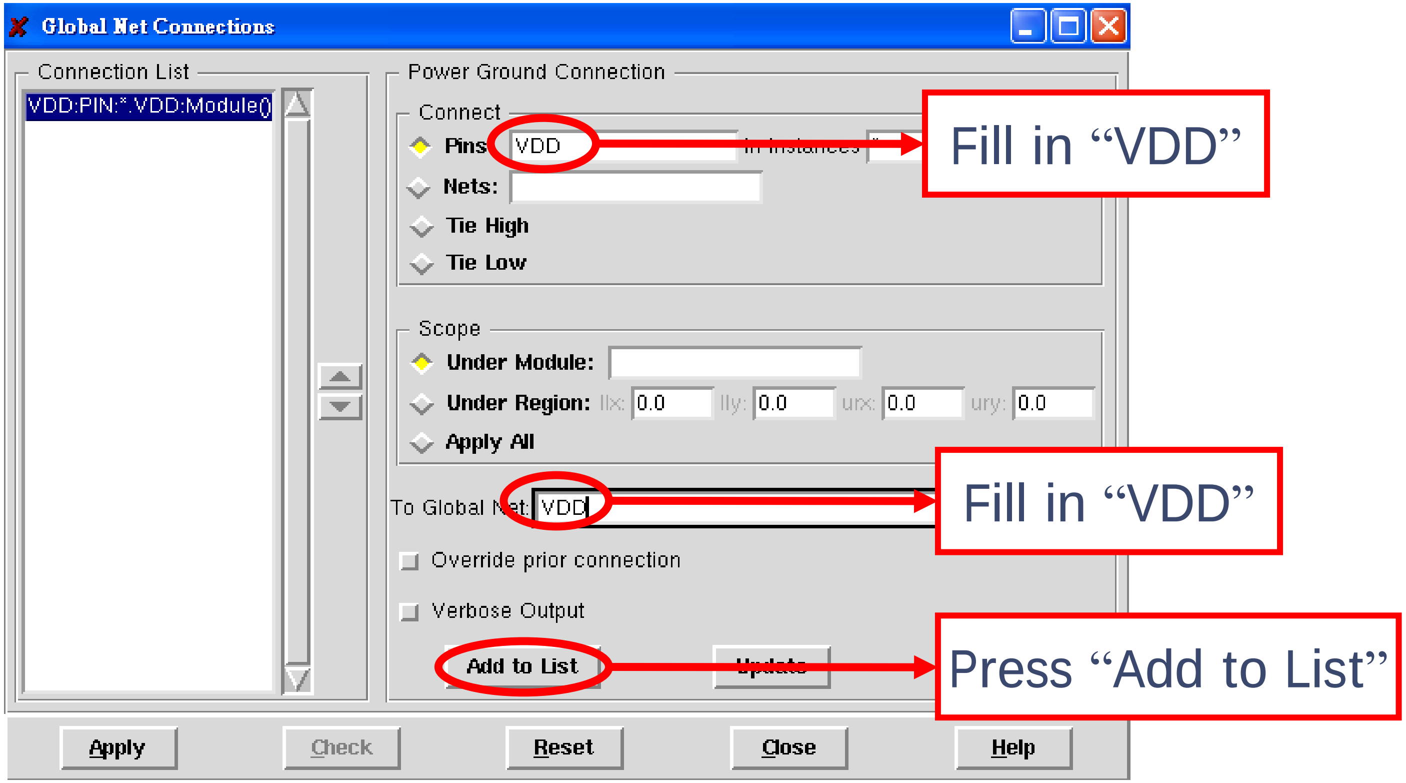
Toggle Rate Scale Factor: 1.0

Import Your Design (6/6)



Global Net Connect (1/2)

- Floorplan → Connect Global Net



Global Net Connections

Connection List

VDD:PIN:*.VDD:Module()

Power Ground Connection

Connect

- ● Pins: VDD in instances: *
- ○ Nets:
- ○ Tie High
- ○ Tie Low

Scope

- ● Under Module:
- ○ Under Region: llx: 0.0 lly: 0.0 urx: 0.0 ury: 0.0
- ○ Apply All

To Global Net: VDD

□ Override prior connection

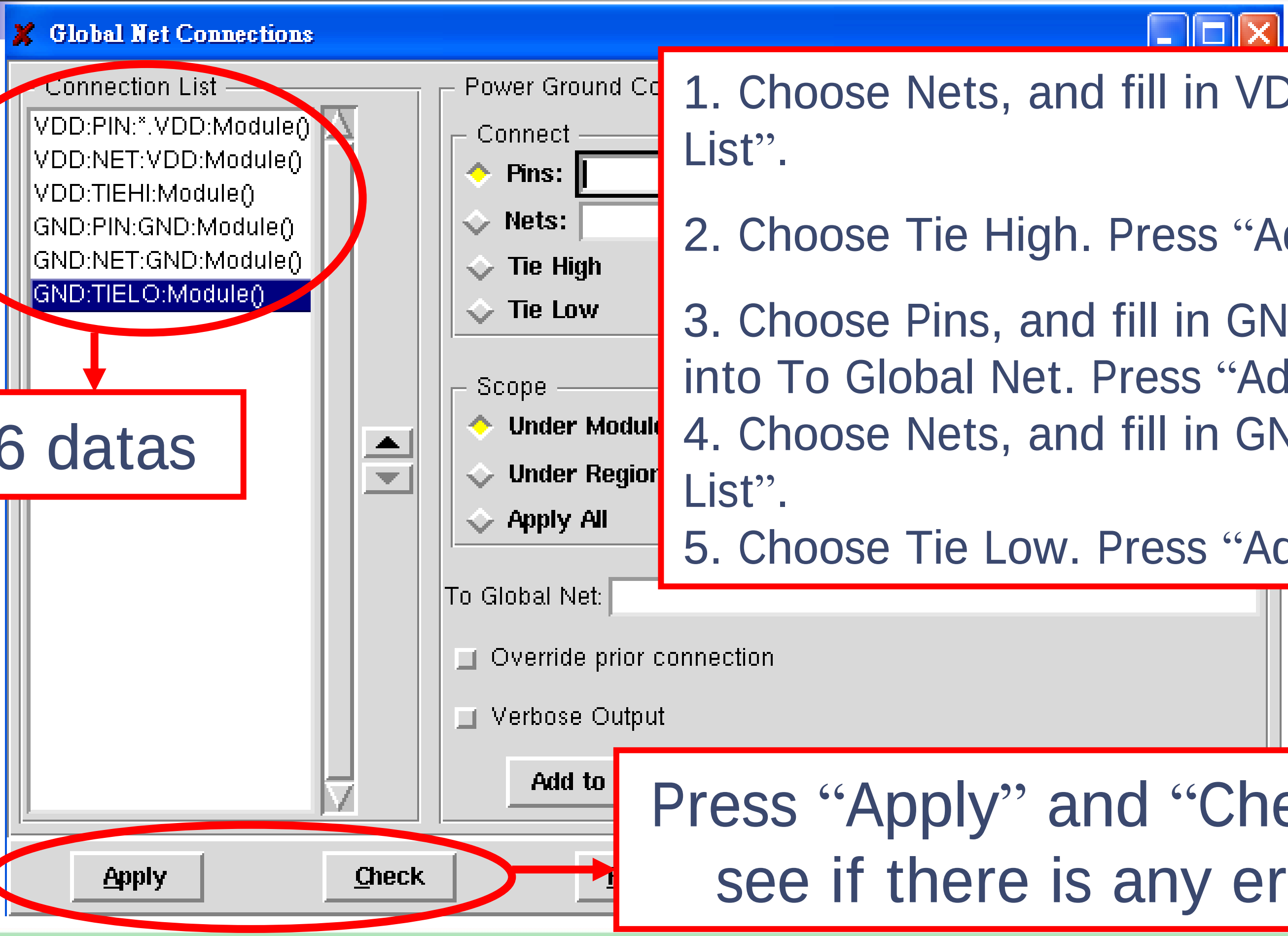
□ Verbose Output

Fill in "VDD"

Fill in "VDD"

Press "Add to List"

Global Net Connect (2/2)



Global Net Connections

Connection List

VDD:PIN:*.VDD:Module()
VDD:NET:VDD:Module()
VDD:TIEHI:Module()
GND:PIN:GND:Module()
GND:NET:GND:Module()
GND:TIELO:Module()

6 datas

1. Choose Nets, and fill in VDD. Press “Add to List”.

2. Choose Tie High. Press “Add to List”

3. Choose Pins, and fill in GND. Fill in GND into To Global Net. Press “Add to List”.
4. Choose Nets, and fill in GND. Press “Add to List”.
5. Choose Tie Low. Press “Add to List”

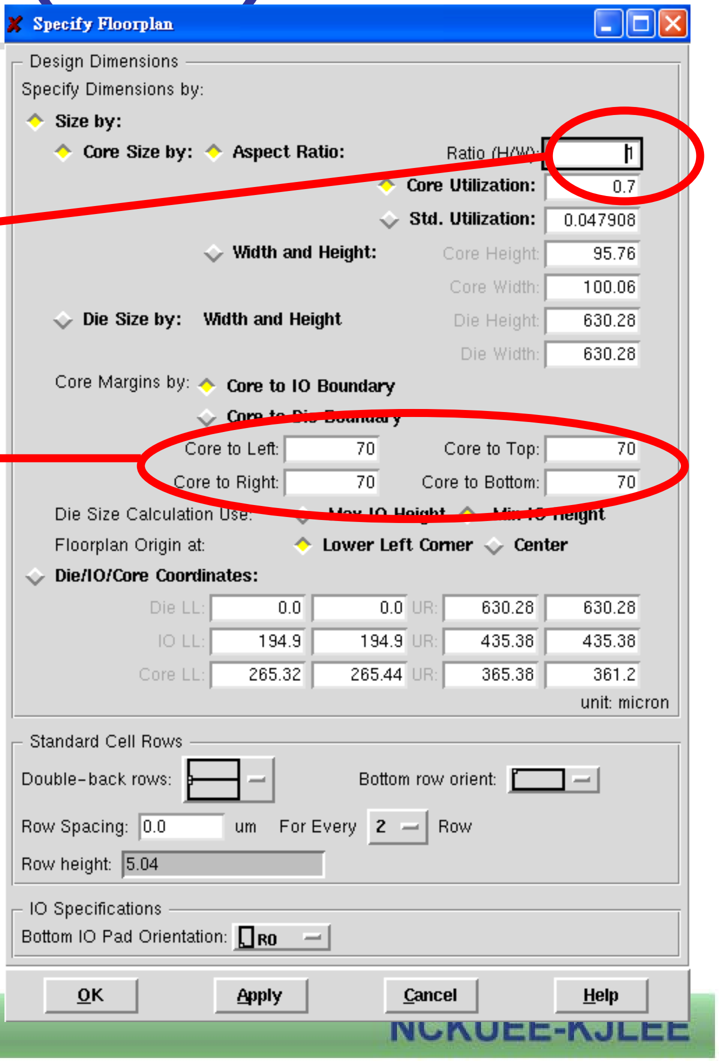
Press “Apply” and “Check”, see if there is any error

Specify Floorplan (1/3)

- Floorplan → Specify Floorplan

Fill in “1” and “0.7”

All fill in “70”



Specify Floorplan

Design Dimensions

Specify Dimensions by:

◆ Size by:

◆ Core Size by: ◆ Aspect Ratio: Ratio (H/W): 1

◆ Core Utilization: 0.7

◇ Std. Utilization: 0.047908

◇ Width and Height: Core Height: 95.76

Core Width: 100.06

◇ Die Size by: Width and Height Die Height: 630.28

Die Width: 630.28

Core Margins by: ◆ Core to IO Boundary

◇ Core to Die Boundary

Core to Left: 70 Core to Top: 70

Core to Right: 70 Core to Bottom: 70

Die Size Calculation Use: ◇ Max IO Height ◆ Min IO Height

Floorplan Origin at: ◆ Lower Left Corner ◇ Center

◇ Die/IO/Core Coordinates:

Die LL:	0.0	0.0	UR:	630.28	630.28
IO LL:	194.9	194.9	UR:	435.38	435.38
Core LL:	265.32	265.44	UR:	365.38	361.2

unit: micron

Standard Cell Rows

Double-back rows: Bottom row orient:

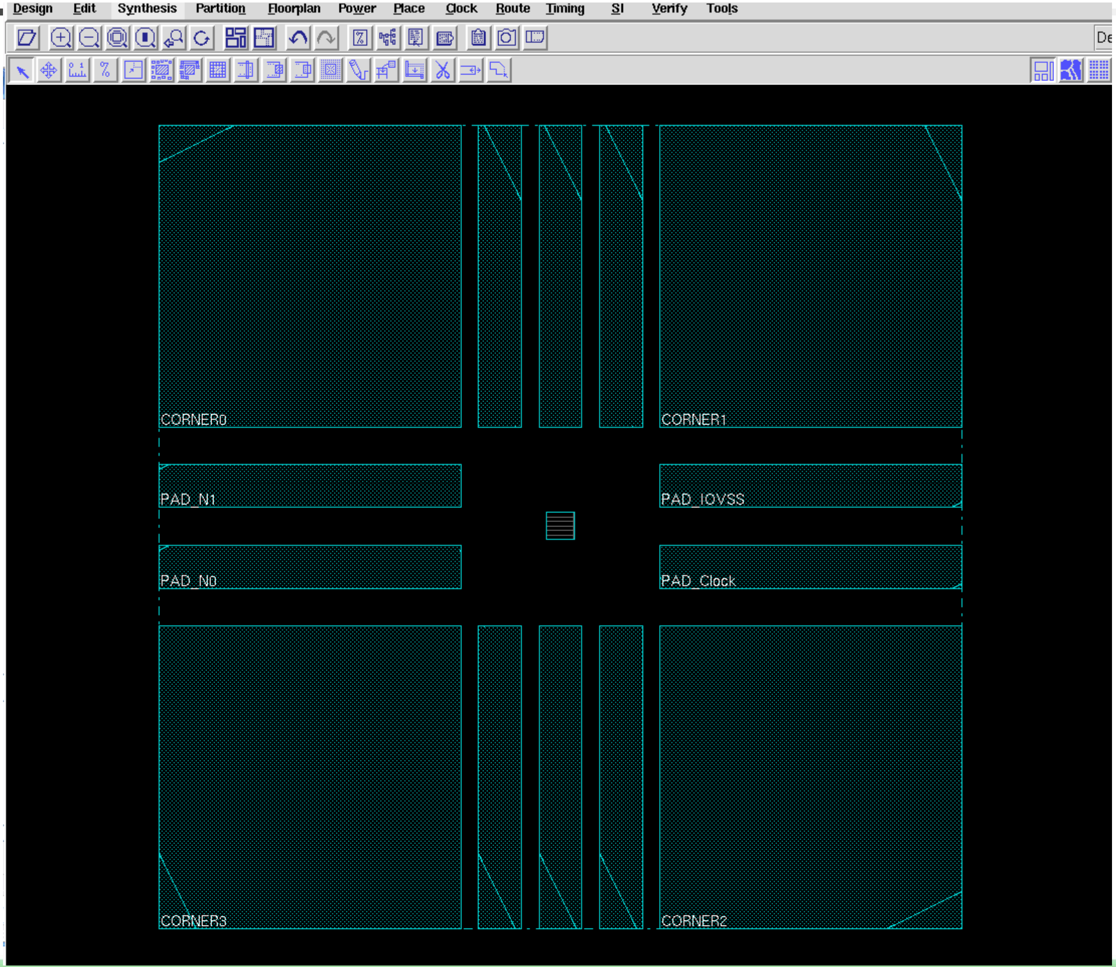
Row Spacing: 0.0 um For Every 2 Row

Row height: 5.04

IO Specifications

Bottom IO Pad Orientation: R0

Specify Floorplan (2/3)

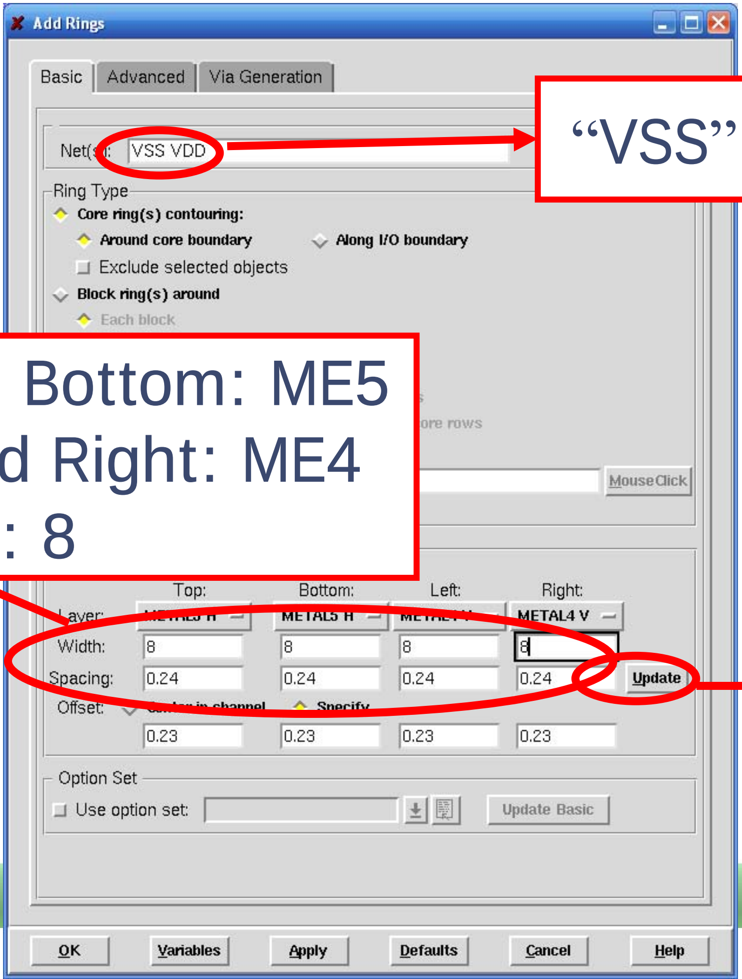


Specify Floorplan (3/3)

- Design → Save Design

Powerplan (1/6)

- Power → Power Planning → Add Rings



Add Rings

Net(s): VSS VDD

Ring Type

● Core ring(s) contouring:

● Around core boundary ○ Along I/O boundary

□ Exclude selected objects

○ Block ring(s) around

● Each block

	Top:	Bottom:	Left:	Right:
Layer:	METAL5 H	METAL5 H	METAL4 V	METAL4 V
Width:	8	8	8	8
Spacing:	0.24	0.24	0.24	0.24
Offset: ○ Center in channel ● Specify				
	0.23	0.23	0.23	0.23

Option Set

□ Use option set:

"VSS" and "VDD" only

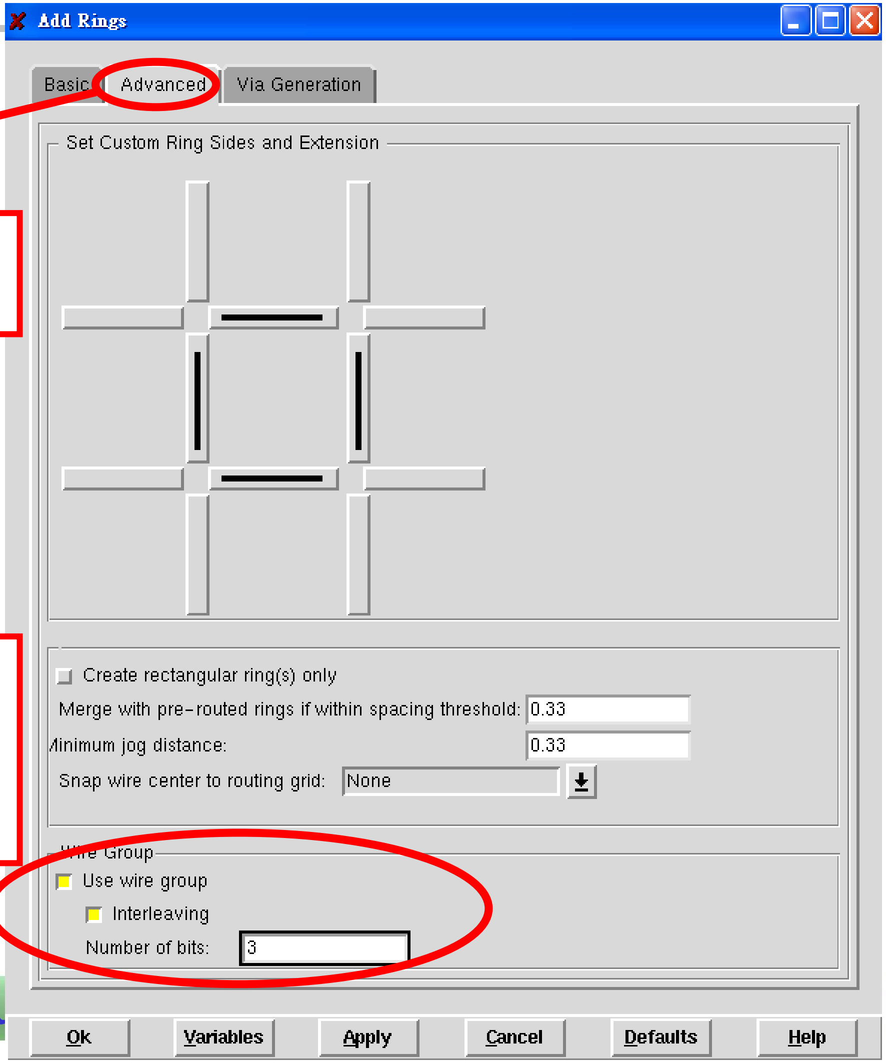
Layer of Top and Bottom: ME5
Layer of Left and Right: ME4
Width: 8

Press "Update"

Powerplan (2/6)

Switch to “Advanced”

Choose “Use wire group”
And “Interleaving”
Number of bits: 3



□ Create rectangular ring(s) only

Merge with pre-routed rings if within spacing threshold: 0.33

/inimum jog distance: 0.33

Snap wire center to routing grid: None

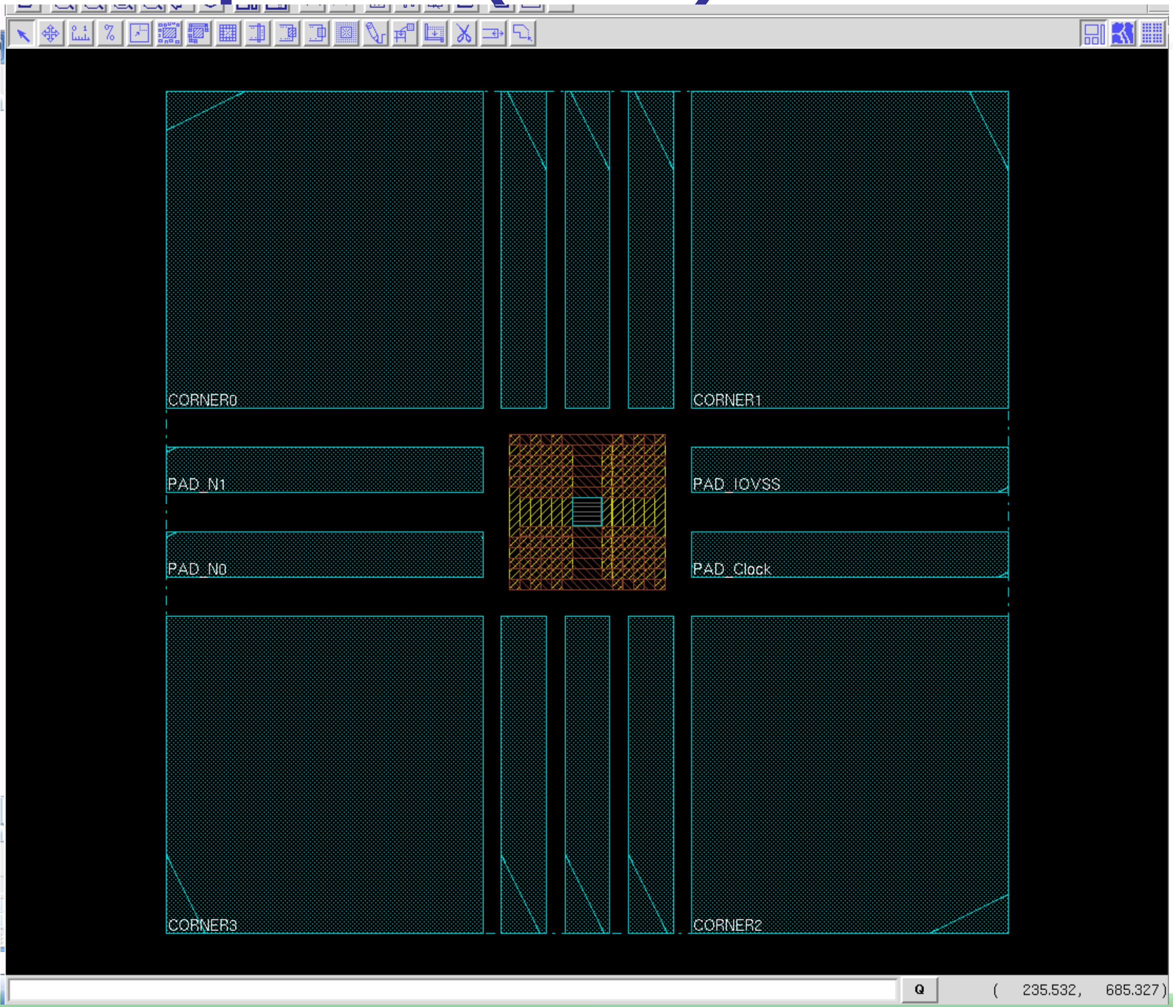
Wire Group

☑ Use wire group

☑ Interleaving

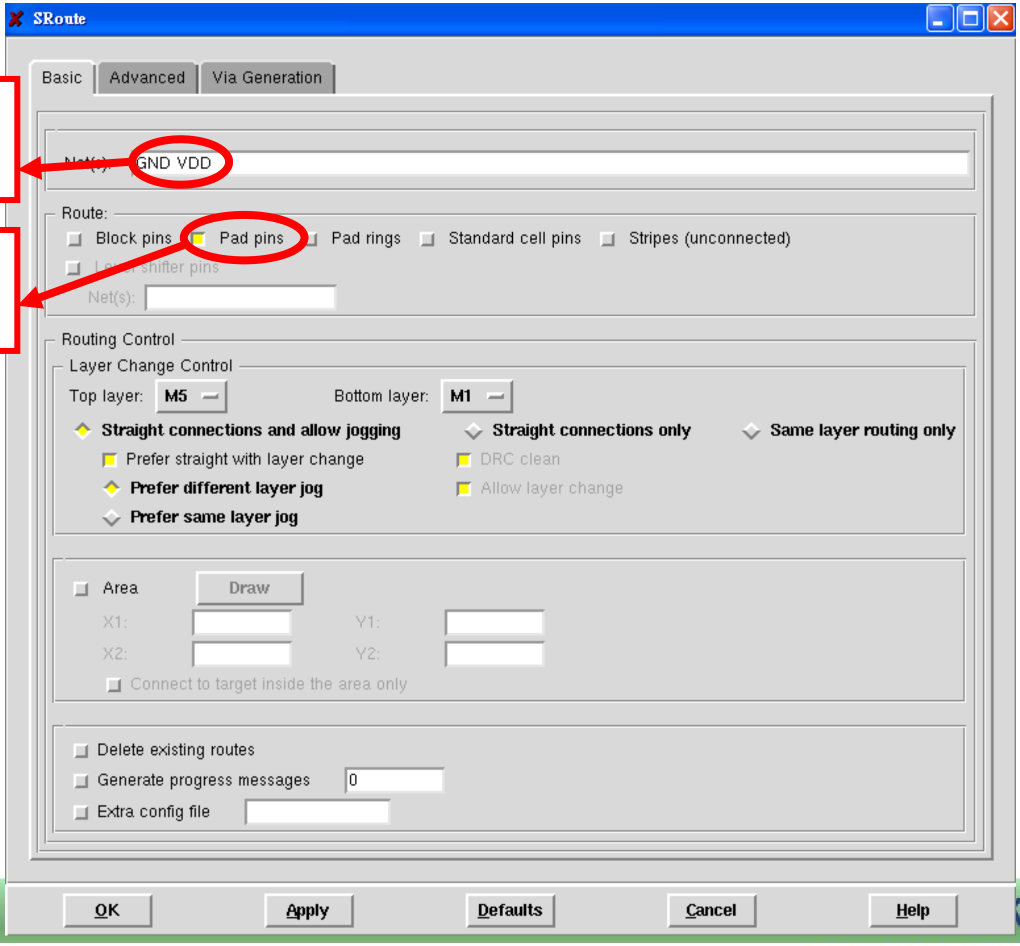
Number of bits: 3

Powerplan (3/6)



Powerplan (4/6)

- Route → Special Route



SRoute

Basic | Advanced | Via Generation

Net(s): GND VDD

Route:

□ Block pins ☑ Pad pins □ Pad rings □ Standard cell pins □ Stripes (unconnected)

□ Level shifter pins

Net(s):

Routing Control

Layer Change Control

Top layer: M5 Bottom layer: M1

● Straight connections and allow jogging ○ Straight connections only ○ Same layer routing only

☑ Prefer straight with layer change ☑ DRC clean

● Prefer different layer jog ☑ Allow layer change

○ Prefer same layer jog

□ Area Draw

X1: Y1:

X2: Y2:

□ Connect to target inside the area only

□ Delete existing routes

□ Generate progress messages 0

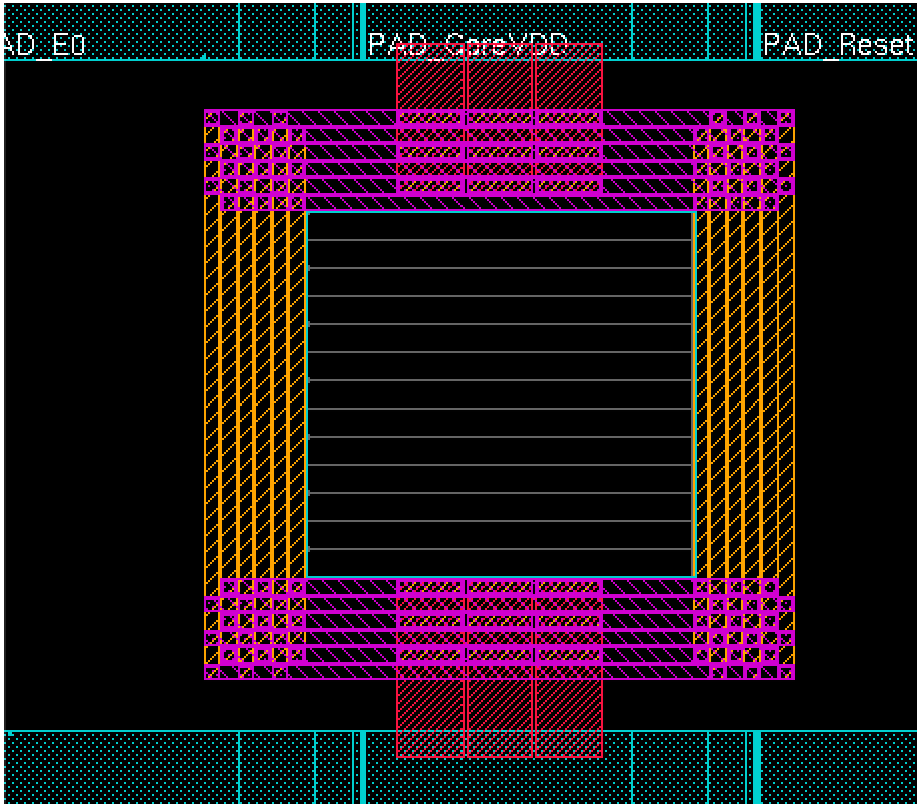
□ Extra config file

OK | Apply | Defaults | Cancel | Help

“VSS” and “VDD” only

“Pad pins” only

Powerplan (5/6)

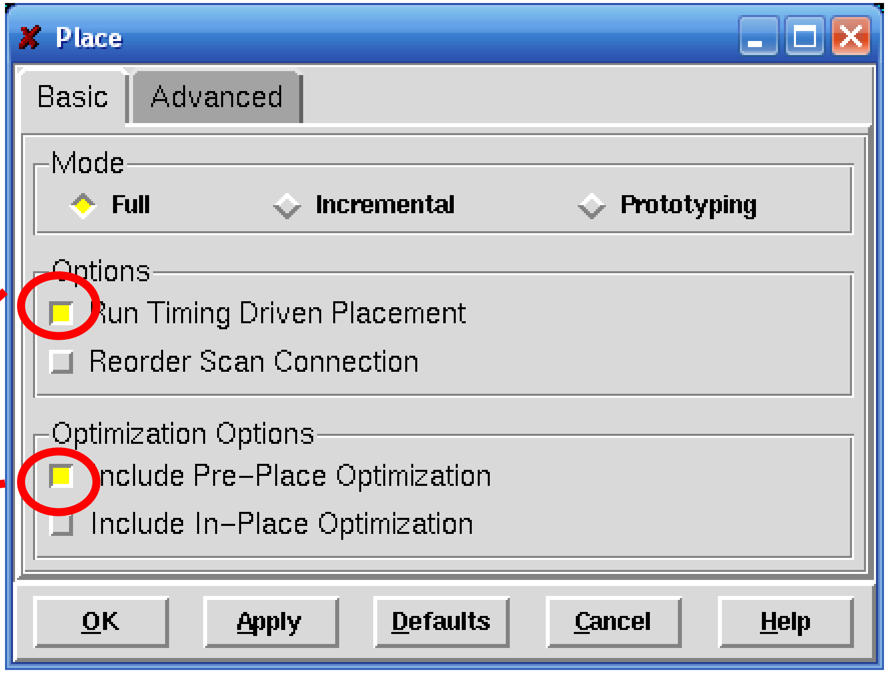


Powerplan (6/6)

- Design → Save Design

Place (1/2)

- Place → Standard Cell And Blocks
- Prototyping: fast
- Full: complete



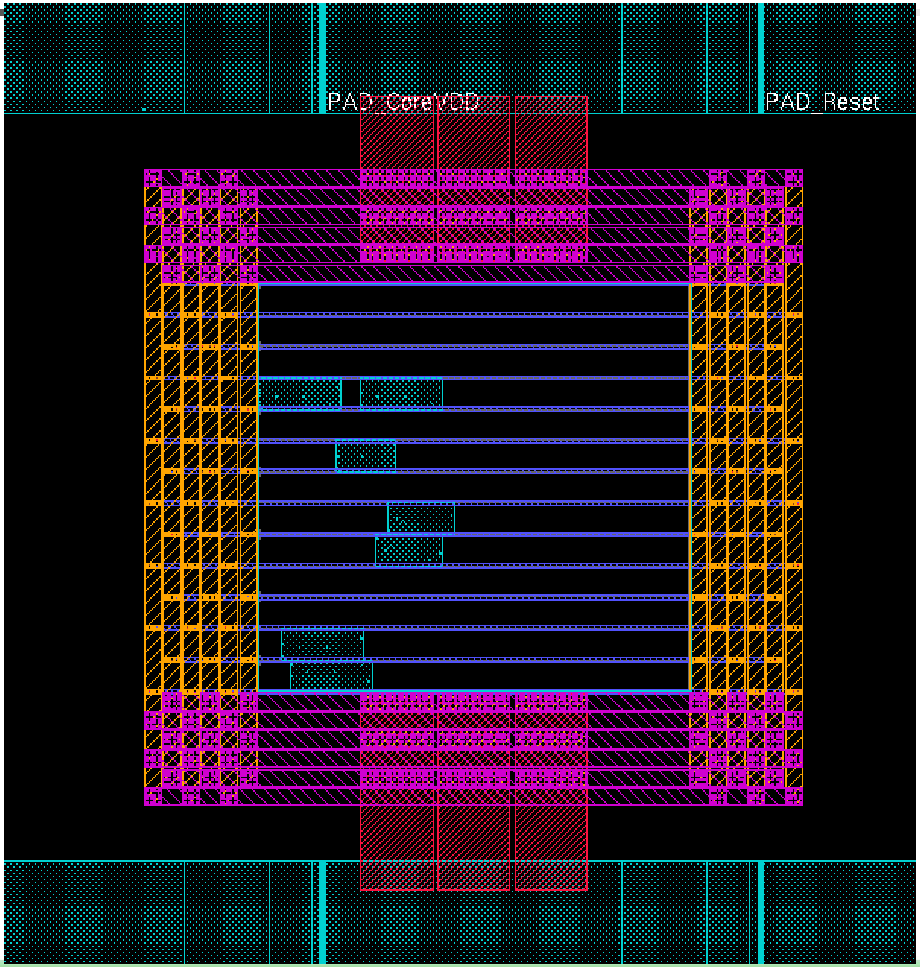
Mode
● Full ○ Incremental ○ Prototyping

Options
☑ Run Timing Driven Placement
□ Reorder Scan Connection

Optimization Options
☑ Include Pre–Place Optimization
□ Include In–Place Optimization

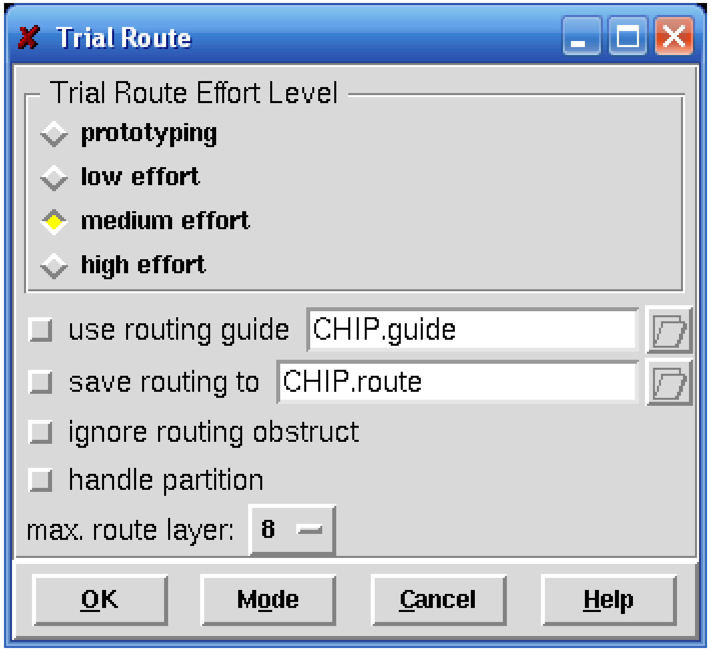
Choose two of these

Place (2/2)



Trail Route (1/2)

- Route → Trail Route



Trial Route

Trial Route Effort Level

○ prototyping

○ low effort

● medium effort

○ high effort

□ use routing guide CHIP.guide

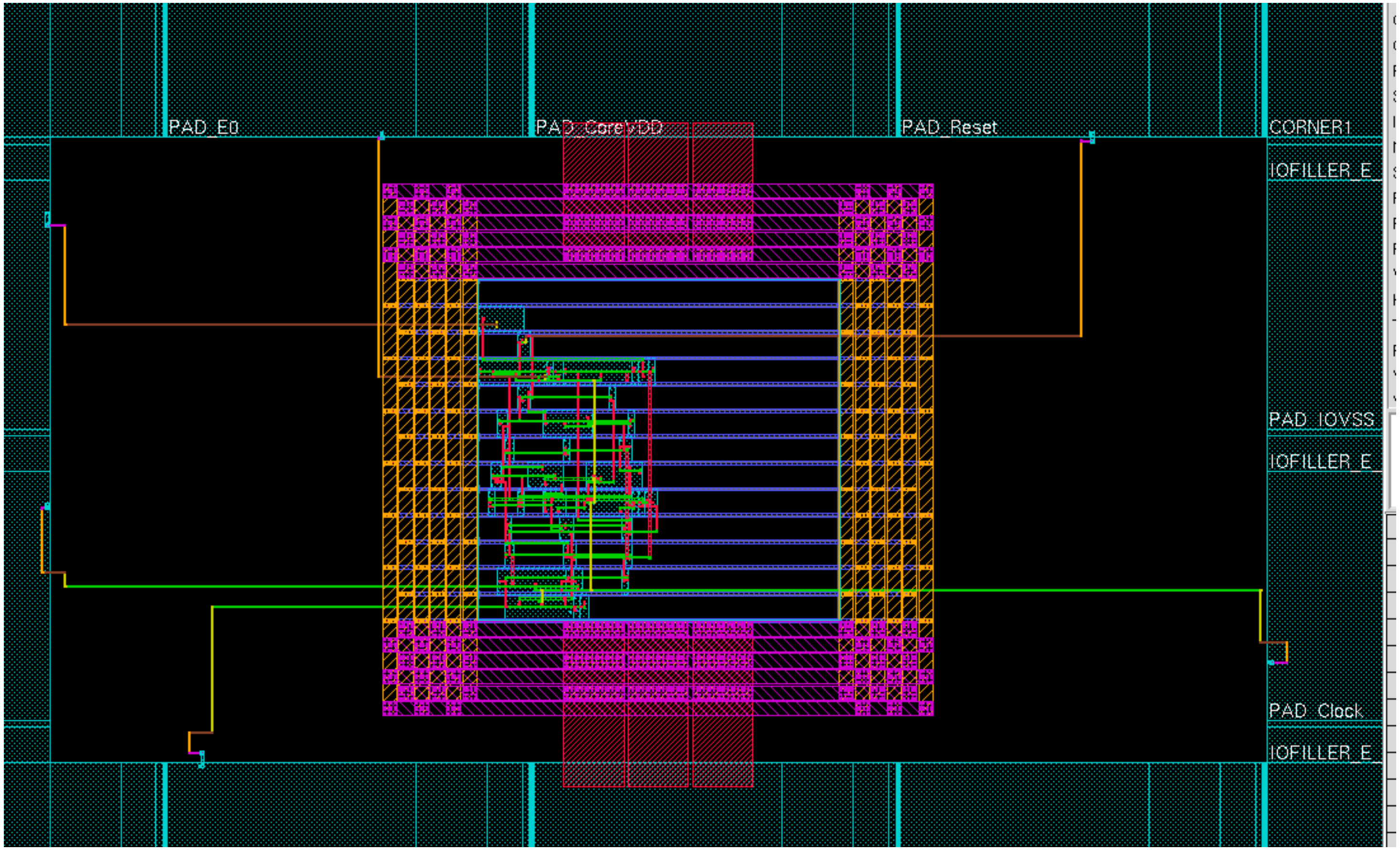
□ save routing to CHIP.route

□ ignore routing obstruct

□ handle partition

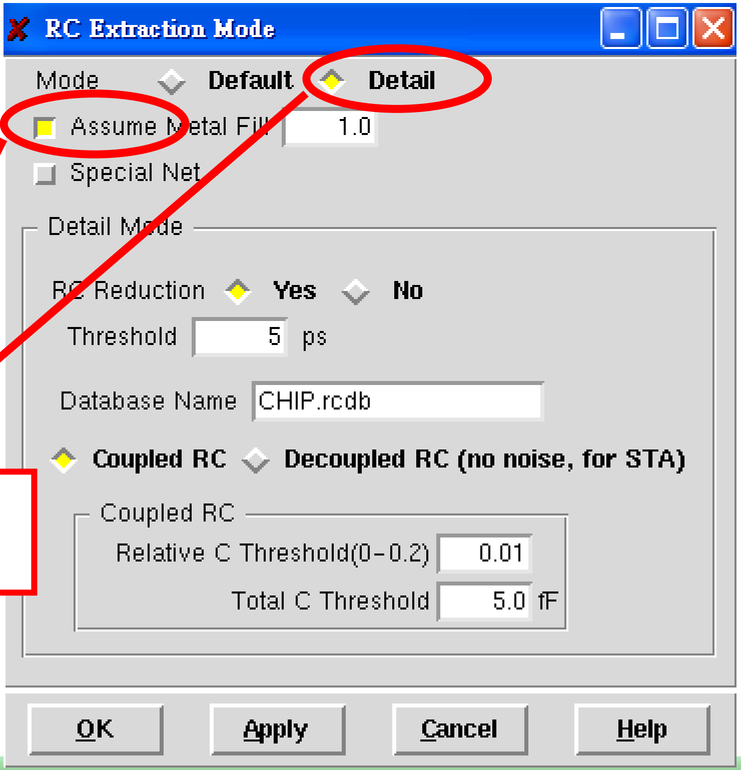
max. route layer: 8

Trail Route (2/2)



Trail Route: Time Analysis (1/2)

- Timing → Specify Analysis Condition →Specify RC Extraction Mode



RC Extraction Mode

Mode ○ Default ● Detail

☑ Assume Metal Fill 1.0

□ Special Net

Detail Mode

RC Reduction ● Yes ○ No

Threshold 5 ps

Database Name CHIP.rcdb

● Coupled RC ○ Decoupled RC (no noise, for STA)

Coupled RC

Relative C Threshold(0-0.2) 0.01

Total C Threshold 5.0 fF

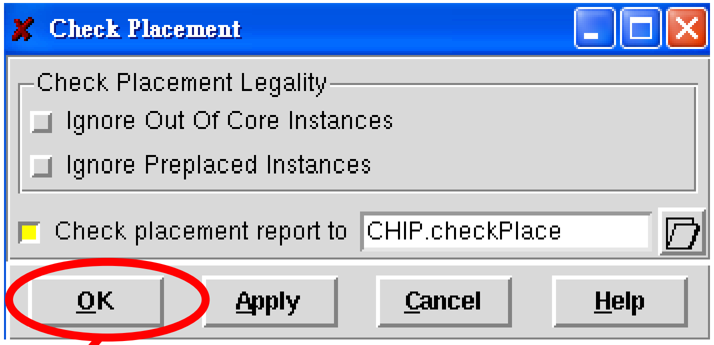
Choose two of these

Trail Route: Time Analysis (2/2)

- Timing → Extract RC, and press OK
- Timing → Timing Analysis, and press OK
- Terminal → Check the Slack
- If there is some negative Timing Slack, you can “Timing →Optimization”
- If still negative, you must synthesis again

Check

- Place → Check Placement



Check Placement

Check Placement Legality

□ Ignore Out Of Core Instances

□ Ignore Preplaced Instances

☑ Check placement report to CHIP.checkPlace

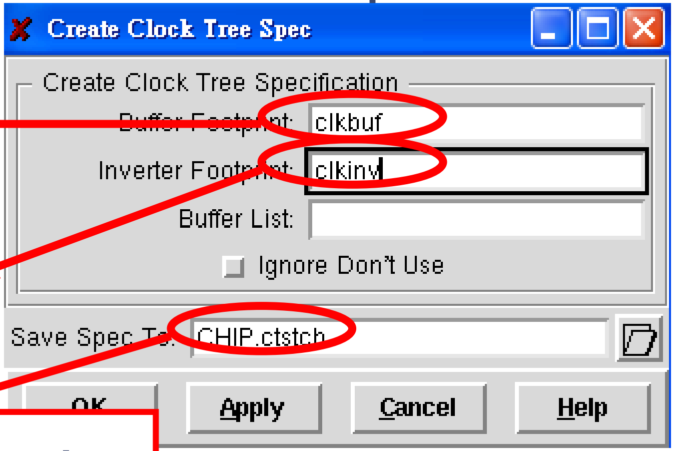
Press OK

Trail Route

- Design → Save Design

Clock Tree Synthesis (1/3)

- Clock → Create Clock Tree Spec



Create Clock Tree Spec

Create Clock Tree Specification

Buffer Footprint: clkbuf

Inverter Footprint: clkinv

Buffer List:

□ Ignore Don't Use

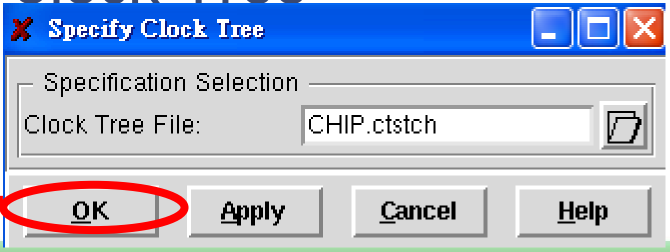
Save Spec To: CHIP.ctstch

Fill in “clkbuf”

Fill in “clkinv”

Save to “CHIP.ctstch”

- Clock → Specify Clock Tree



Specify Clock Tree

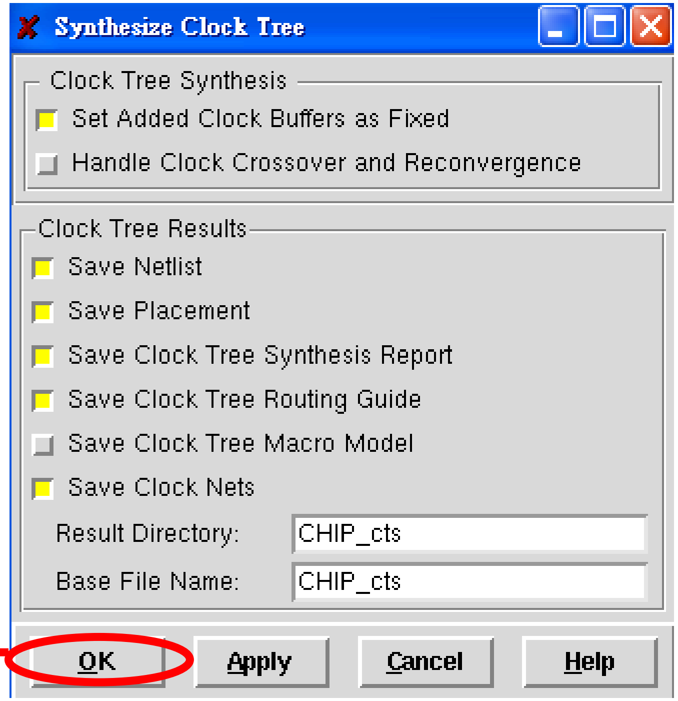
Specification Selection

Clock Tree File: CHIP.ctstch

Press OK

Clock Tree Synthesis (2/3)

- Clock → Synthesize Clock tree



Synthesize Clock Tree

Clock Tree Synthesis

☑ Set Added Clock Buffers as Fixed

☐ Handle Clock Crossover and Reconvergence

Clock Tree Results

☑ Save Netlist

☑ Save Placement

☑ Save Clock Tree Synthesis Report

☑ Save Clock Tree Routing Guide

☐ Save Clock Tree Macro Model

☑ Save Clock Nets

Result Directory: CHIP_cts

Base File Name: CHIP_cts

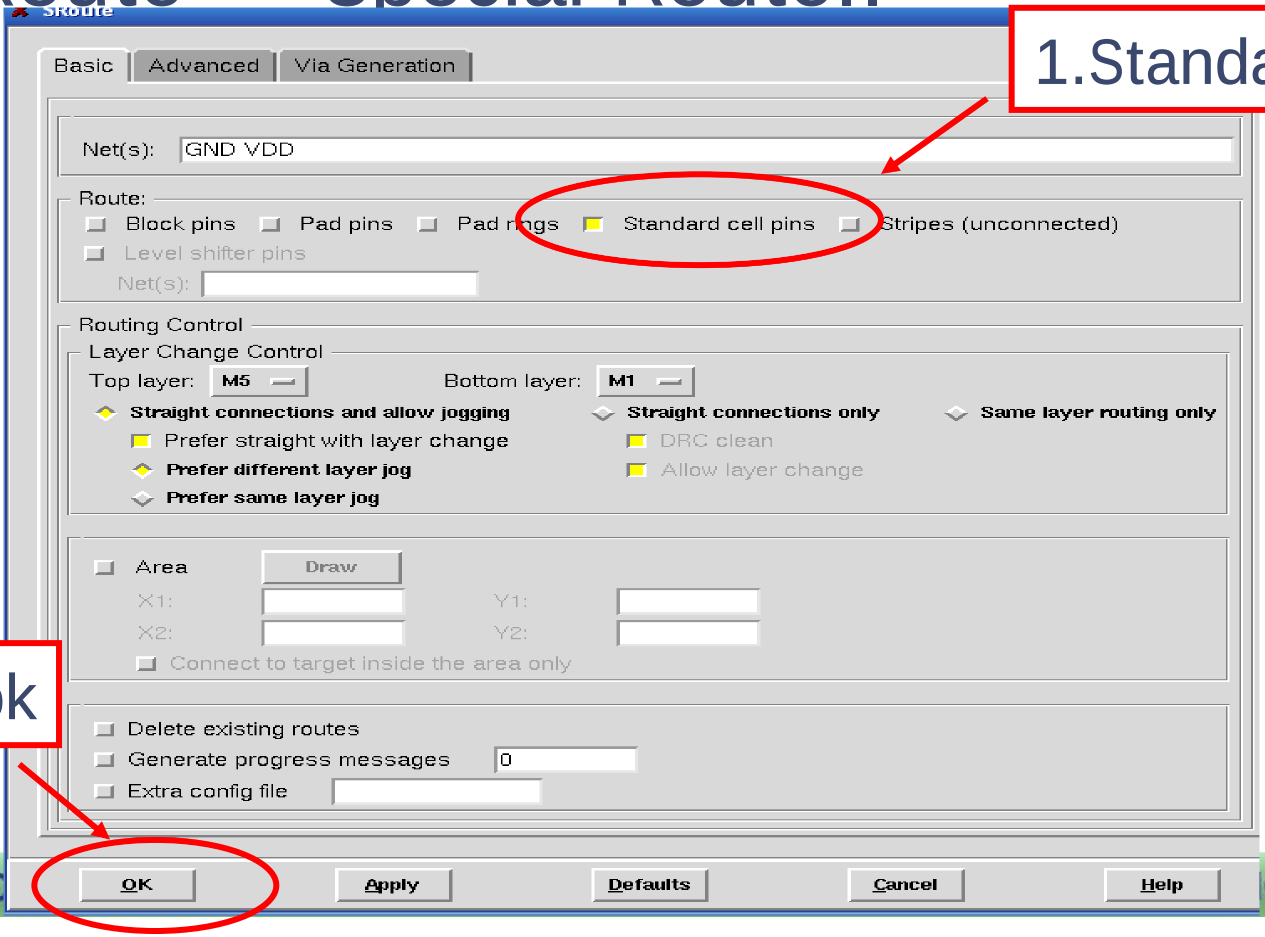
Press OK

Clock Tree Synthesis (3/3)

- Design → Save Design

Connect follpower

- Route → Special Route..



Net(s): GND VDD

Route:

□ Block pins □ Pad pins □ Pad rings ☑ Standard cell pins □ Stripes (unconnected)

□ Level shifter pins

Net(s):

Routing Control

Layer Change Control

Top layer: M5 Bottom layer: M1

● Straight connections and allow jogging ○ Straight connections only ○ Same layer routing only

☑ Prefer straight with layer change ☑ DRC clean

● Prefer different layer jog ☑ Allow layer change

○ Prefer same layer jog

□ Area Draw

X1: Y1:

X2: Y2:

□ Connect to target inside the area only

□ Delete existing routes

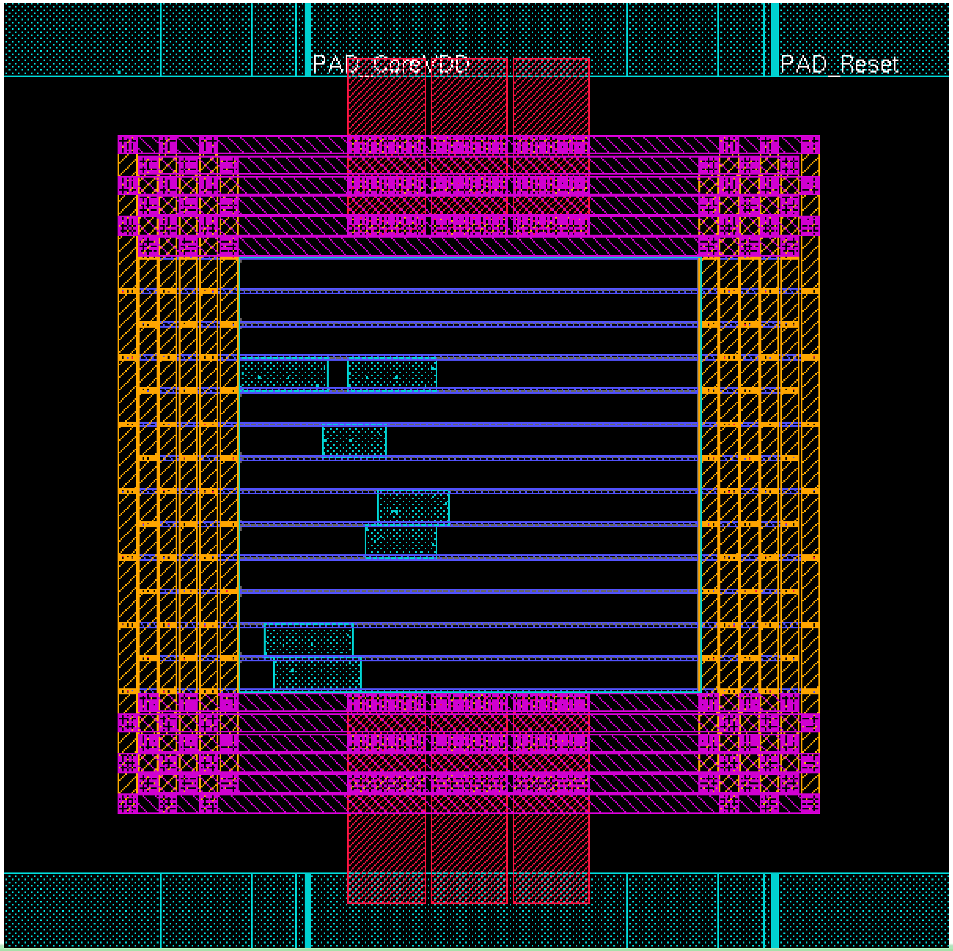
□ Generate progress messages 0

□ Extra config file

1.Standard cell pins

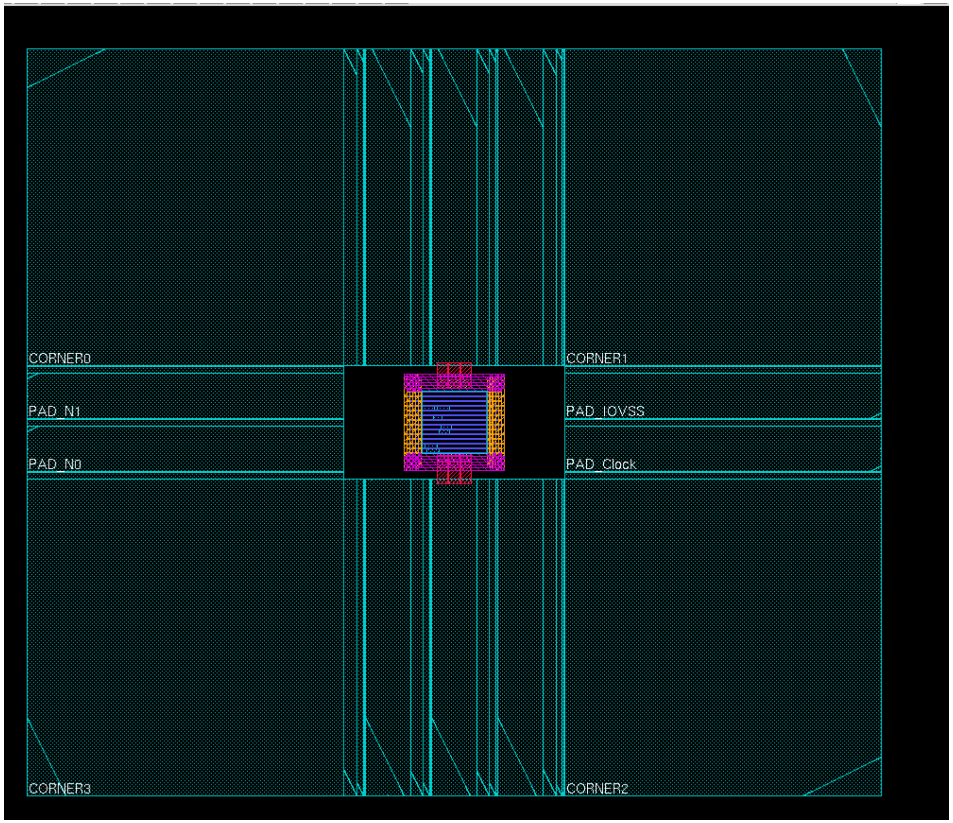
2.pass ok

Connect follpower



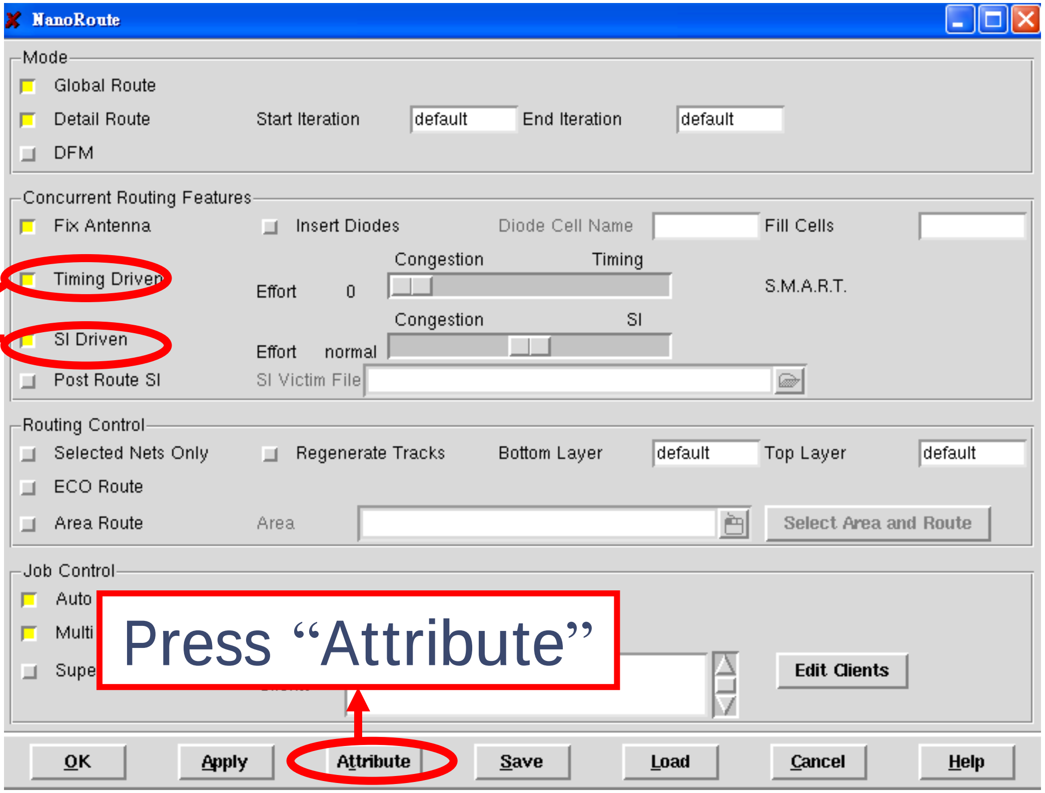
Add io filler

Type “source addIoFiller_tpz.cmd” in terminal



NanoRoute (1/2)

- Route → NanoRoute → Route..



NanoRoute

Mode
- ☑ Global Route
- ☑ Detail Route — Start Iteration: default — End Iteration: default
- □ DFM

Concurrent Routing Features
- ☑ Fix Antenna — □ Insert Diodes — Diode Cell Name: — Fill Cells:
- ☑ Timing Driven — Effort: 0 — Congestion ↔ Timing — S.M.A.R.T.
- ☑ SI Driven — Effort: normal — Congestion ↔ SI
- □ Post Route SI — SI Victim File:

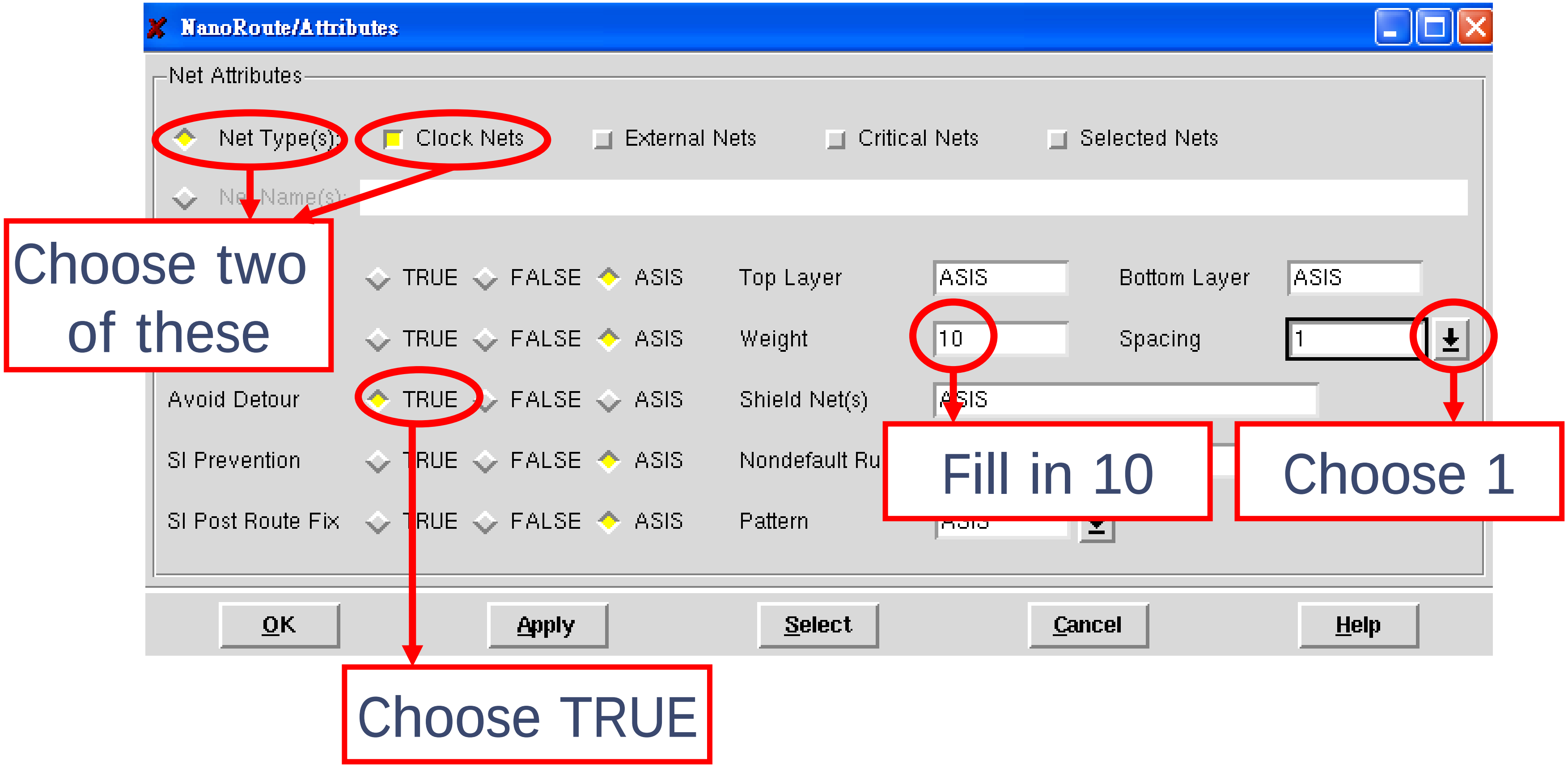
Routing Control
- □ Selected Nets Only — □ Regenerate Tracks — Bottom Layer: default — Top Layer: default
- □ ECO Route
- □ Area Route — Area: — Select Area and Route

Job Control
- ☑ Auto
- ☑ Multi
- □ Supe

Choose two of these

Press “Attribute”

NanoRoute (2/2)



NanoRoute/Attributes

Net Attributes

◆ Net Type(s): ☑ Clock Nets □ External Nets □ Critical Nets □ Selected Nets

◇ Ne Name(s):

	◇ TRUE	◇ FALSE	◆ ASIS	Top Layer	ASIS	Bottom Layer	ASIS
	◇ TRUE	◇ FALSE	◆ ASIS	Weight	10	Spacing	1
Avoid Detour	◆ TRUE	◇ FALSE	◇ ASIS	Shield Net(s)	ASIS		
SI Prevention	◇ TRUE	◇ FALSE	◆ ASIS	Nondefault Ru			
SI Post Route Fix	◇ TRUE	◇ FALSE	◆ ASIS	Pattern	ASIS		

Choose two of these

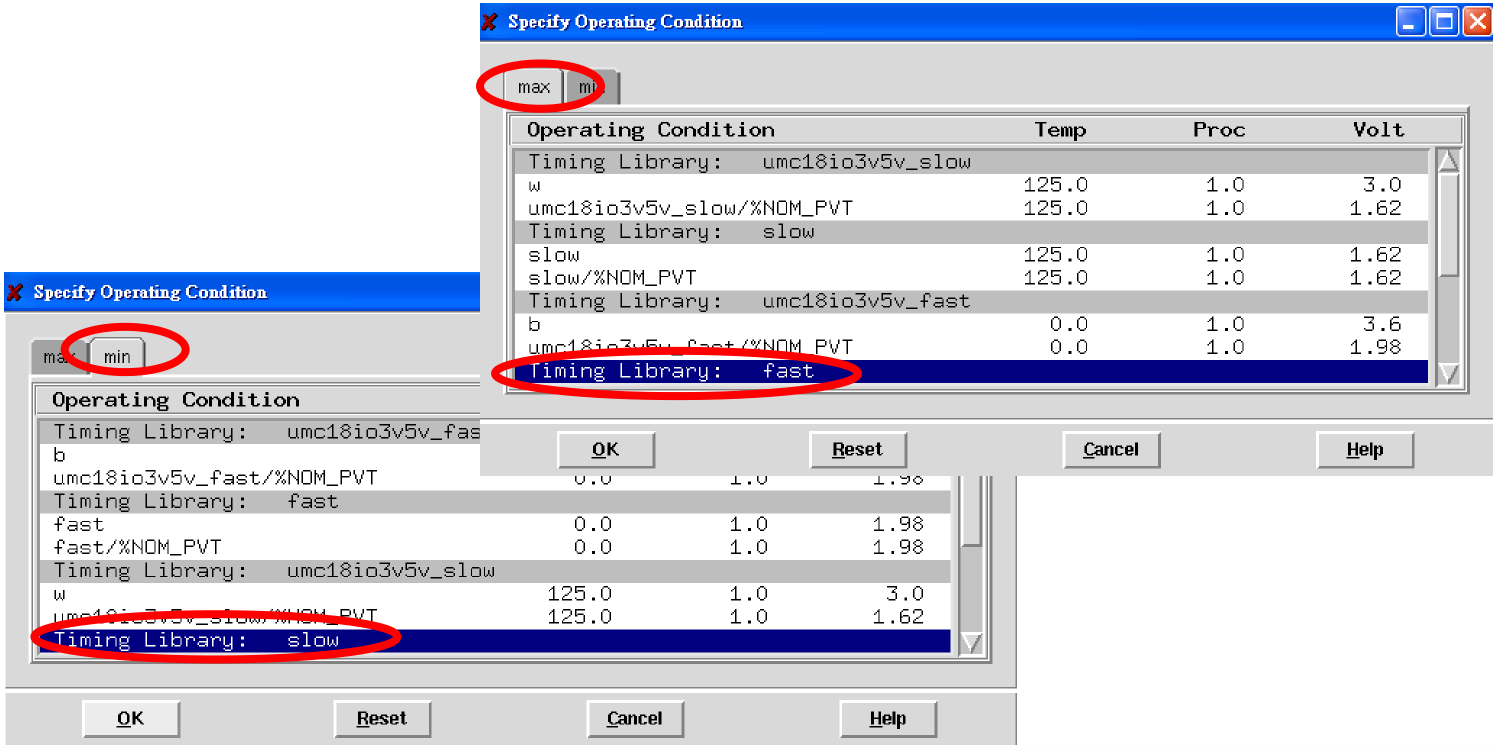
Fill in 10

Choose 1

Choose TRUE

Timing Analysis (1/4)

- Timing → Specify Analysis Condition → Specify Operating Condition/PVT



Specify Operating Condition

Operating Condition	Temp	Proc	Volt
Timing Library: umc18io3v5v_slow			
w	125.0	1.0	3.0
umc18io3v5v_slow/%NOM_PVT	125.0	1.0	1.62
Timing Library: slow			
slow	125.0	1.0	1.62
slow/%NOM_PVT	125.0	1.0	1.62
Timing Library: umc18io3v5v_fast			
b	0.0	1.0	3.6
umc18io3v5v_fast/%NOM_PVT	0.0	1.0	1.98
Timing Library: fast			

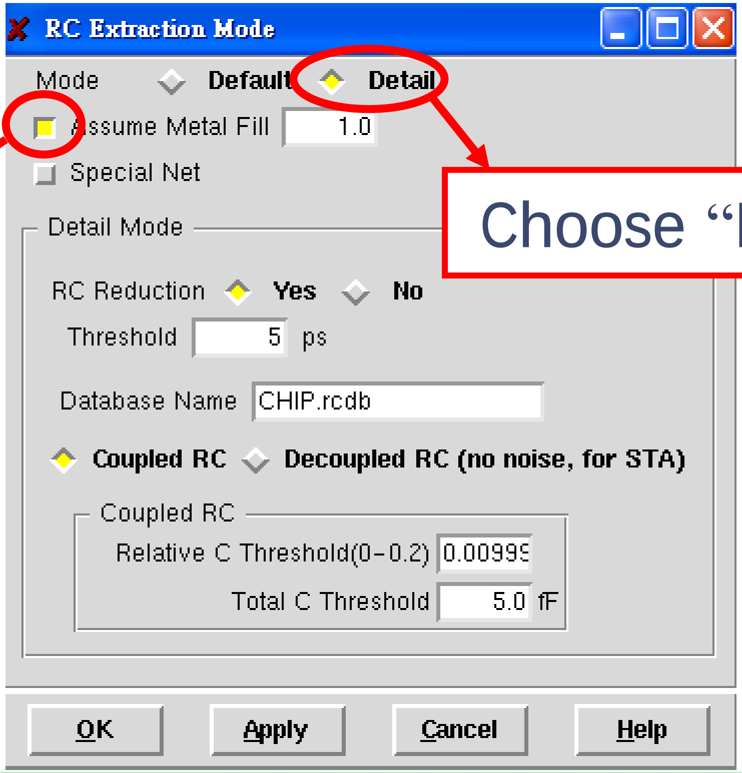
Specify Operating Condition

Operating Condition			
Timing Library: umc18io3v5v_fas			
b			
umc18io3v5v_fast/%NOM_PVT	0.0	1.0	1.98
Timing Library: fast			
fast	0.0	1.0	1.98
fast/%NOM_PVT	0.0	1.0	1.98
Timing Library: umc18io3v5v_slow			
w	125.0	1.0	3.0
umc18io3v5v_slow/%NOM_PVT	125.0	1.0	1.62
Timing Library: slow			

Timing Analysis (2/4)

- Timing → Specify Analysis Condition → Specify RC Extraction Mode

Choose "Assume Metal Fill"



RC Extraction Mode

Mode ○ Default ● Detail

☑ Assume Metal Fill 1.0

□ Special Net

Detail Mode

RC Reduction ● Yes ○ No

Threshold 5 ps

Database Name CHIP.rcdb

● Coupled RC ○ Decoupled RC (no noise, for STA)

Coupled RC

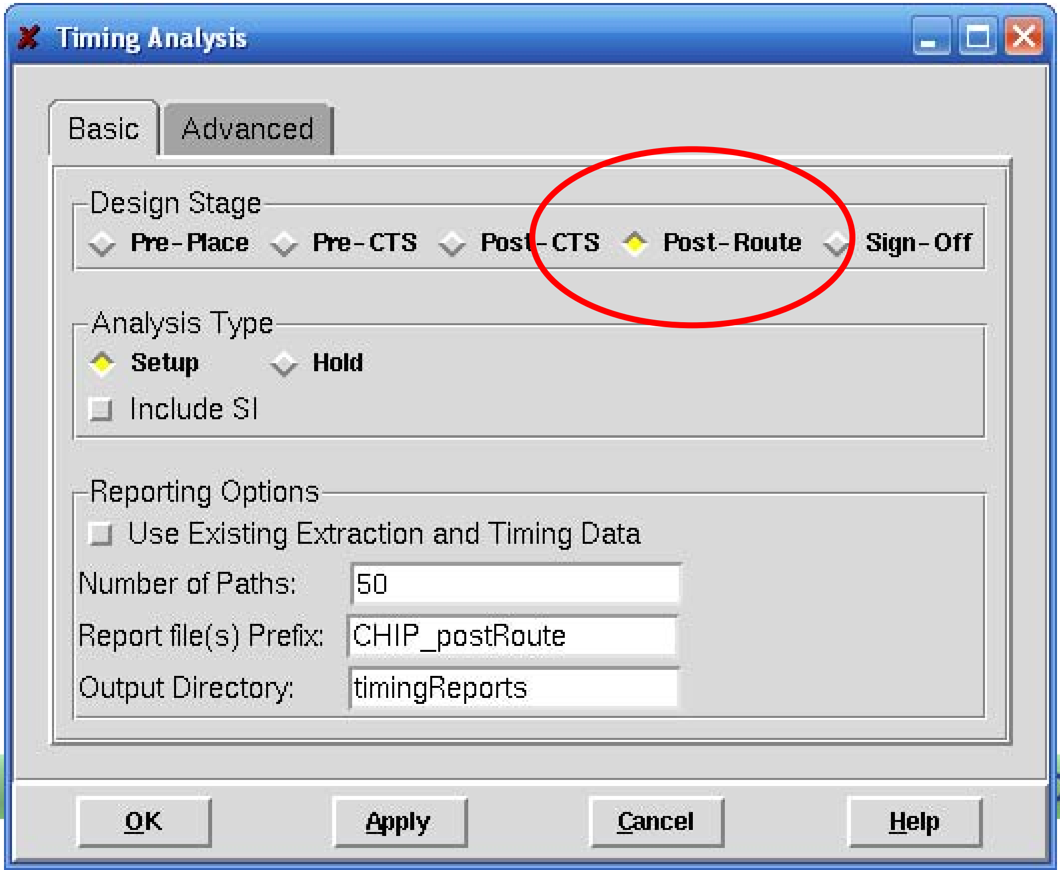
Relative C Threshold(0-0.2) 0.00999

Total C Threshold 5.0 fF

Choose "Detail"

Timing Analysis (3/4)

- Timing → Extract RC → OK
- Timing → Timing Analysis



Design Stage

○ Pre-Place ○ Pre-CTS ○ Post-CTS ● Post-Route ○ Sign-Off

Analysis Type

● Setup ○ Hold

□ Include SI

Reporting Options

□ Use Existing Extraction and Timing Data

Number of Paths: 50

Report file(s) Prefix: CHIP_postRoute

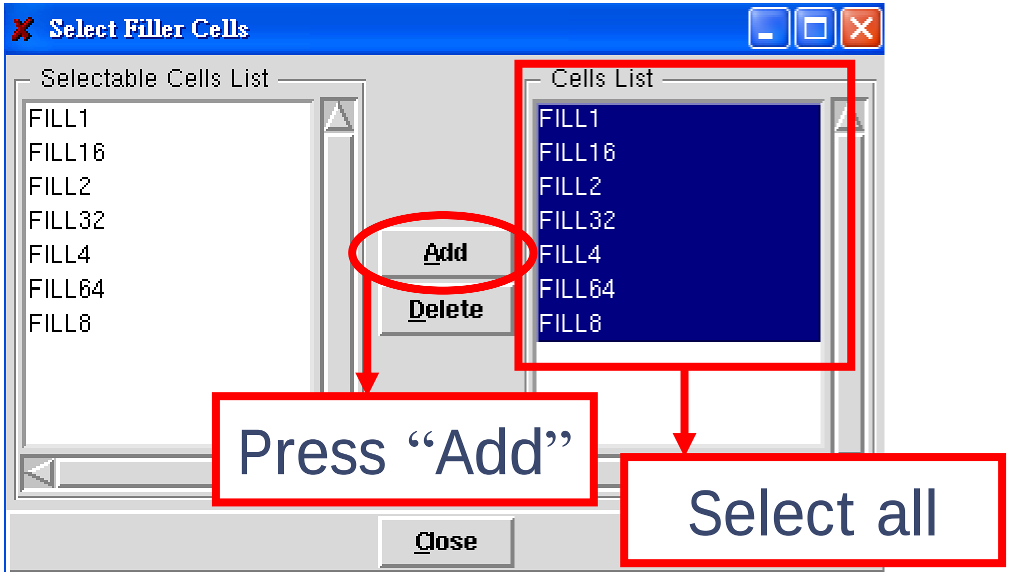
Output Directory: timingReports

Timing Analysis (4/4)

- Terminal → Check the Slack
- If there is some negative Timing Slack, you can “Timing →Optimization”
- If still negative, you must synthesis again

Add Filler (1/2)

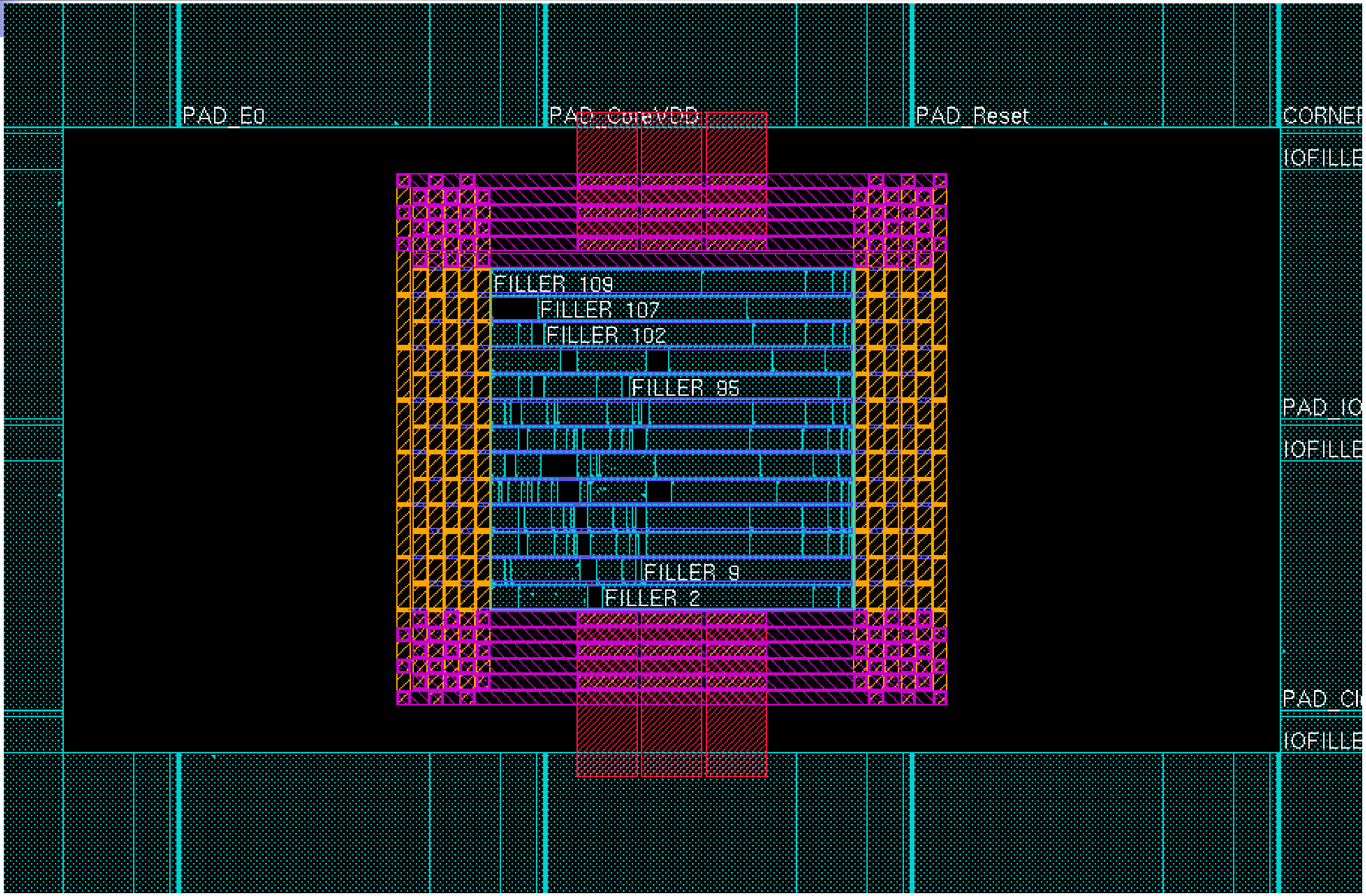
- Place → Filler → Add..
- In Add Filler Form, press “select”



Press “Add”

Select all

Add Filler (2/2)



Check

- Verify → Connectivity
- Verify → Geometry
- Place → Check placement

Save Design

- Step 1. Design → Save Design
  - File name : finish.enc
- Step 2. Design → Save → GDS
  - Output Stream File : CHIP.gds
  - Map File : streamOut.map
  - Units 2000 → 1000
- Step 3. Design → Save → Netlist
  - File name : CHIP_lvs.v
- Step 4. Design → Save → DEF
  - File name : CHIP.def
- Step 5. Design → Exit

Prepare for Verification

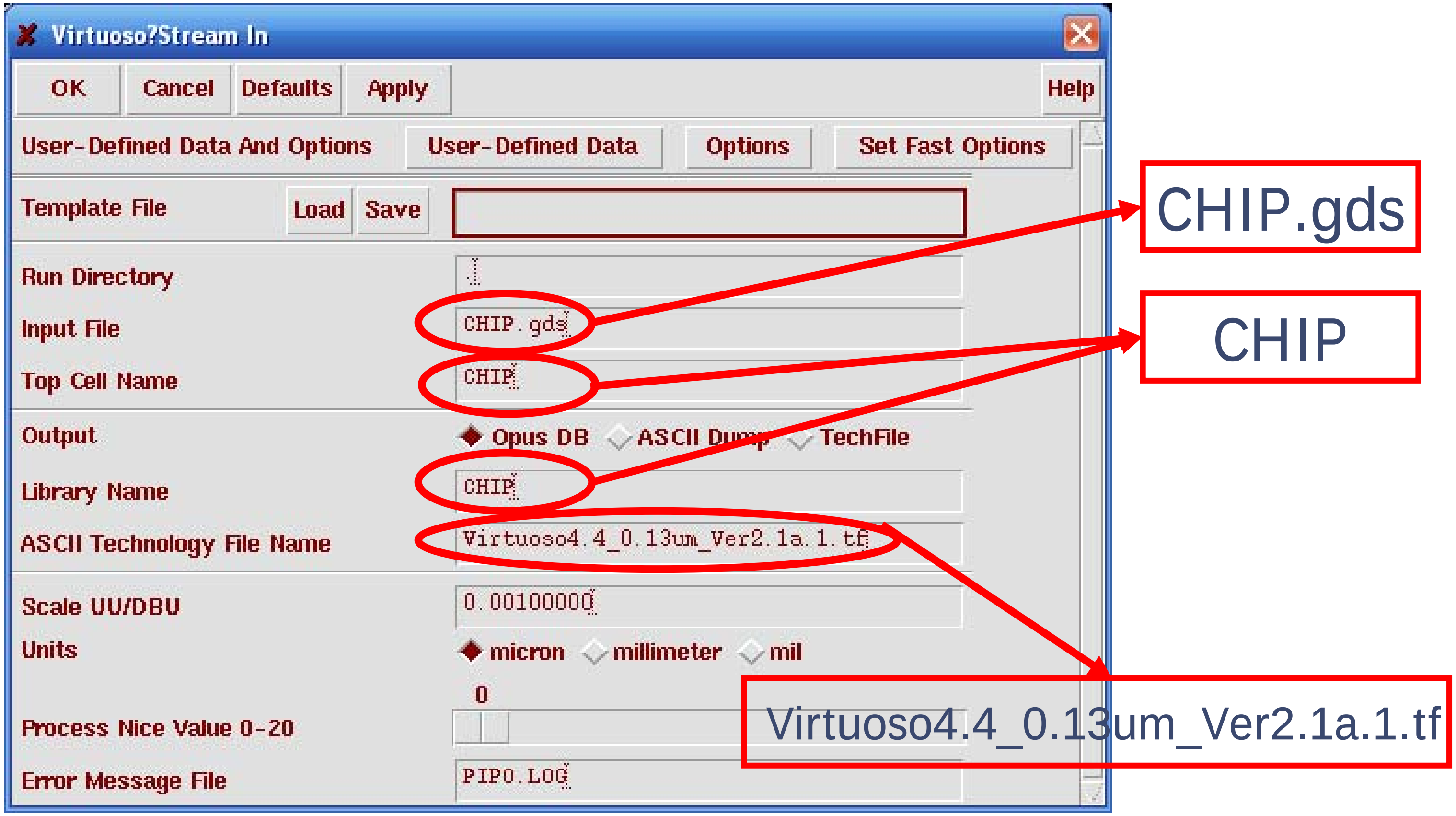
- Stream In Design
- Stream Out Design

Stream In Design (1/3)

- Copy CHIP.gds to directory icfb
- Source the file
  - source /usr/cad/mentor/CIC/calibre.cshrc
  - icfb &
- Workstation
  - /Library/icfb directory

Stream In Design (2/3)

- File → Import → Stream



Template File

Run Directory .

Input File CHIP.gds

Top Cell Name CHIP

Output ● Opus DB ○ ASCII Dump ○ TechFile

Library Name CHIP

ASCII Technology File Name Virtuoso4.4_0.13um_Ver2.1a.1.tf

Scale UU/DBU 0.00100000

Units ● micron ○ millimeter ○ mil

Process Nice Value 0-20 0

Error Message File PIPO.LOG

CHIP.gds

CHIP

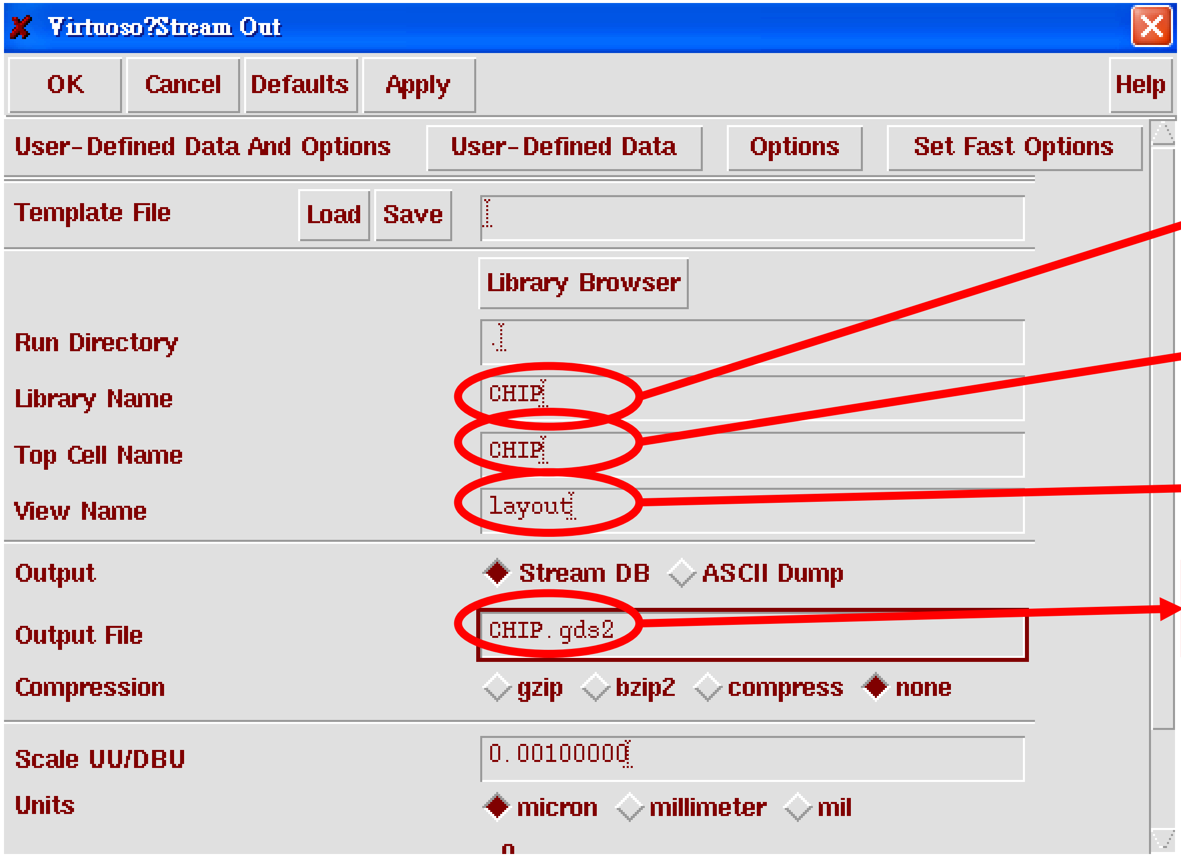
Virtuoso4.4_0.13um_Ver2.1a.1.tf

Stream In Design (3/3)

- File → Import → Stream
  - Input File: tpz013g3.gds
    (the file is in the GDSII directory)
  - Top Cell Name: empty
  - Press OK
- File → Import → Stream
  - Input File: tsmc13gfsg_fram.gds
    (the file is in the GDSII directory)
  - Top Cell Name: empty
  - Press OK

Stream Out Design

- File → Export → Stream



Template File

Run Directory .

Library Name CHIP

Top Cell Name CHIP

View Name layout

Output ● Stream DB ○ ASCII Dump

Output File CHIP.gds2

Compression ○ gzip ○ bzip2 ○ compress ● none

Scale UU/DBU 0.00100000

Units ● micron ○ millimeter ○ mil

CHIP

CHIP

layout

CHIP.gds2

Design Check

- DRC
- LVS

DRC

- Copy CHIP.gds2 from directory icfb to verify/drc
- Edit file Calibre-drc-cur
  - Replace Layout PATH to Layout PATH “CHIP.gds2”
  - Replace Layout PRIMARY to Layout PRIMARY “CHIP”
- Execute Calibre
  - calibre -drc -hier Calibre-drc-cur
- Check result
  - Open file “drc.summary”, it should be no errors

LVS (1/3)

- Copy CHIP.gds2 to directory LVS
- Copy CHIP_lvs.v to directory LVS
- Transform CHIP_lvs.v to spice format
  - v2lvs -v CHIP_lvs.v -l tsmc13gfsg_fram_lvs.v -o CHIP.spi -s tsmc13gfsg_fram_lvs.spi –s1 VDD –s0 GND

LVS (2/3)

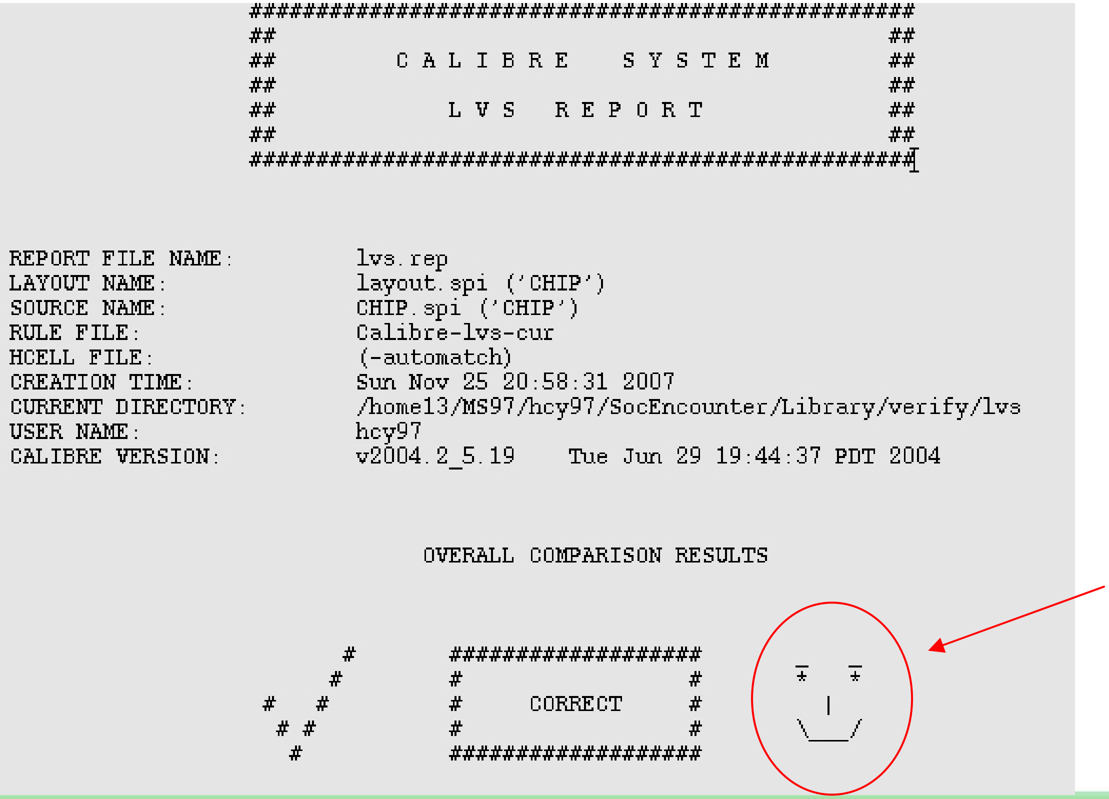
- Edit file Calibre-lvs-cur
  - Replace SOURCE PRIMARY to SOURCE PRIMARY “CHIP”
  - Replace SOURCE PATH to SOURCE PATH “CHIP.spi”
  - Replace Layout PRIMARY to Layout PRIMARY “CHIP”
  - Replace Layout PATH to Layout PATH “CHIP.gds2”

LVS (3/3)

- Execute Calibre
  - calibre -lvs -spice layout.spi -hier -auto Calibre-lvs-cur

Result

- Check result
  - Open file “lvs.report”



```
                   ##################################################
                   ##                                              ##
                   ##         C A L I B R E    S Y S T E M         ##
                   ##                                              ##
                   ##             L V S    R E P O R T             ##
                   ##                                              ##
                   ##################################################



REPORT FILE NAME:          lvs.rep
LAYOUT NAME:               layout.spi ('CHIP')
SOURCE NAME:               CHIP.spi ('CHIP')
RULE FILE:                 Calibre-lvs-cur
HCELL FILE:                (-automatch)
CREATION TIME:             Sun Nov 25 20:58:31 2007
CURRENT DIRECTORY:         /home13/MS97/hcy97/SocEncounter/Library/verify/lvs
USER NAME:                 hcy97
CALIBRE VERSION:           v2004.2_5.19    Tue Jun 29 19:44:37 PDT 2004



                             OVERALL COMPARISON RESULTS



                          #       ###################        _   _
                         #        #                 #        *   *
                    #   #         #     CORRECT     #          |
                     # #          #                 #        \___/
                      #           ###################
```

If there is a smile, the result of LVS is correct